# A Bandwidth-Adaptive Preamplifier

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***Abstract*—We propose an adaptive microphone preamplifier that adjusts its power consumption according to the input signal's bandwidth. A chip prototype of the adaptive preamplifier for speech processing was fabricated in a 0.5-µm CMOS process. The adaptive preamplifier's measured input referred noise is 3 $\mu V_{rms}$ and its total harmonic distortion is −40 dBc for an 80-$mV_{rms}$ input amplitude. These noise and distortion specifications remain virtually constant over the preamplifier's range of bandwidth adaptation. The adaptive preamplifier consumes 65 µW of power. This is achieved with no degradation in speech quality, when compared to a conventional preamplifier of fixed bandwidth, and as measured by the perceptual evaluation of speech quality (PESQ) score.**

***Index Terms*—Adaptive, analog circuit, analog front end (AFE), differential difference amplifier (DDA), envelope detector, hysteretic comparator, low power, microphone, OTA-C filter, power efficient, preamplifier, reconfigurable, sensor interface, subthreshold, wearable sensor.**

## I. Introduction

THERE is a growing interest in consumer biomedical devices that can continually monitor patients' health and provide disease diagnosis [1]–[5]. Ideally, these devices should be wearable and mobile, relying either on batteries or on harvested energy.

A wearable device has a limited power budget. This budget is divided among the analog front end (AFE), the analog-to-digital converter (ADC), the digital signal processor (DSP) and the radio frequency (RF) transceiver, as illustrated in Fig. 1 [6]–[10]. Thanks to data compression and techniques like ultra wide band radio, the energy demands of the RF transceiver are becoming less stringent [8]. In addition, the energy requirements of digital circuits are minimal, due to semiconductor device scaling. Also, the energy efficiency of ADCs is improving, due to advanced architectures that rely more on digital processing [11].

Unfortunately, the AFE still consumes a significant amount of energy. In particular, the preamplifier, which is at the head of the AFE, can easily dominate the power budget of sensor devices.

In this paper, we will present an adaptive preamplifier that automatically adjusts its power consumption according to the bandwidth of the input signal, while maintaining a virtually constant dynamic range. We will describe our implementation of the preamplifier in a speech sensor application and present our measurement results, including the effect of bandwidth adaptation on speech quality.

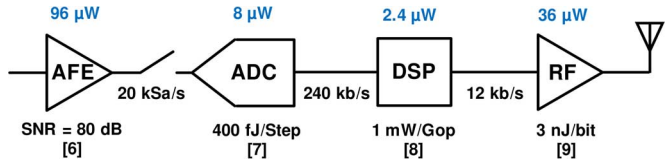


Fig. 1. Power budget of an audio sensor, following the biosensor example of [10]. The power consumption of each building block was derived from the state-of-the-art, scaled to 10 kHz bandwidth and 12 bit resolution. The (delta-sigma) ADC's power consumption includes the decimation filter [7].

Compared to our previous work in [12], the adaptive preamplifier presented in this paper has improved performance of power consumption and noise. Also, in this paper, we present a detailed discussion and analysis of noise and distortion with bandwidth adaptation; circuit implementation details of the bandwidth extractor; and the results of speech quality assessment.

## II. Current Consumption of a Preamplifier

For a preamplifier be able to process a signal at a given bandwidth $BW$, the bias current $I_b$ should be able to charge and discharge the dominant capacitance $C$ fast enough to obtain the required maximum amplitude $A$. Therefore, we have the following relationship:

$$\frac{I_b}{C} \propto BW \cdot A. \tag{1}$$

$C$ is usually determined by the noise requirement, as the preamplifier's integrated noise power is given as:

$$N \propto \frac{kT}{C} \tag{2}$$

where $k$ is Boltzmann's constant, $T$ is the temperature, and $C$ is the dominant capacitance. (2) is valid both when thermal noise is dominant and when the effects of a large $1/f$ noise component are mitigated by chopper stabilization.

Ultimately, we have the following relationship between $I_b$ and $BW$:

$$I_b \propto BW \cdot A \cdot \frac{kT}{N}. \tag{3}$$

### A. Impact of Technology Scaling

In general, circuits designed in newer process technologies would need less current to achieve a given bandwidth. This

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is because smaller channel lengths allow transistors to maintain a high transit frequency, $f_T$, while being pushed into the subthreshold region, where $g_m/I$ efficiency is maximized [13], [14].

However, the low frequency operation of biophysical signal circuits means that the $f_T$ of older processes is still adequate even when the transistors are pushed into subthreshold. So, there is not much benefit to technology scaling for the preamplifier's current consumption. In fact, technology scaling can cause an increase in current consumption due to increased $1/f$ noise and reduced headroom [15].

### B. Adaptive Current Consumption

Following (3), conventional preamplifiers are designed to consume a fixed amount of current, enough to maintain a specified bandwidth and a specified level of input-referred noise. The level of noise is chosen such that when the input is at its minimum amplitude, the signal-to-noise ratio (SNR) will be high enough for the signal to still be useful.

Whenever the input amplitude is much higher than its minimum level, the low fixed noise means that the SNR will be much more than is necessary. This unneeded SNR is achieved at the expense of scarce power resources. To improve power efficiency, some researchers have proposed amplitude-adaptive preamplifiers, which maintain a fixed SNR over the entire input signal amplitude range [16]–[20].

Just like the amplitude, the bandwidth of the input signal is also time-varying. A conventional preamplifier consumes a fixed level of power that is enough to process the maximum possible input signal bandwidth. So, power is unnecessarily wasted whenever the input signal bandwidth is lower than this maximum. We propose a bandwidth-adaptive preamplifier, which adjusts its power consumption to match the bandwidth of the input signal.

Fig. 2 shows the bandwidth-adaptive preamplifier that we designed for a speech sensor. It consists of a bandwidth extractor block and a reconfigurable preamplifier.

The bandwidth extractor detects the bandwidth of the input signal. Then, it sends a control signal to the reconfigurable preamplifier, which adjusts its bandwidth and power consumption accordingly. This adaptive behavior results in a reduction in current consumption from 54 $\mu$A to as low as 8.6 $\mu$A, depending on the required speech quality (see Section VII). The overhead circuitry that makes this possible (bandwidth extractor, reconfigurable components of preamplifier, etc.) consumes less than 3 $\mu$A.

Following are detailed descriptions of the bandwidth extractor and the reconfigurable preamplifier.

## III. Bandwidth Extractor

The input signal enters the bandwidth extractor via a buffer, which drives a bank of 16 bandpass filters with center frequencies spaced logarithmically to cover the frequency band from 200 Hz to 4 kHz (the speech signal's frequency range). The bank of bandpass filters splits the signal into 16 separate channels. In each channel, the envelope of the signal is extracted and sent to a hysteretic comparator. The output of the comparator in the

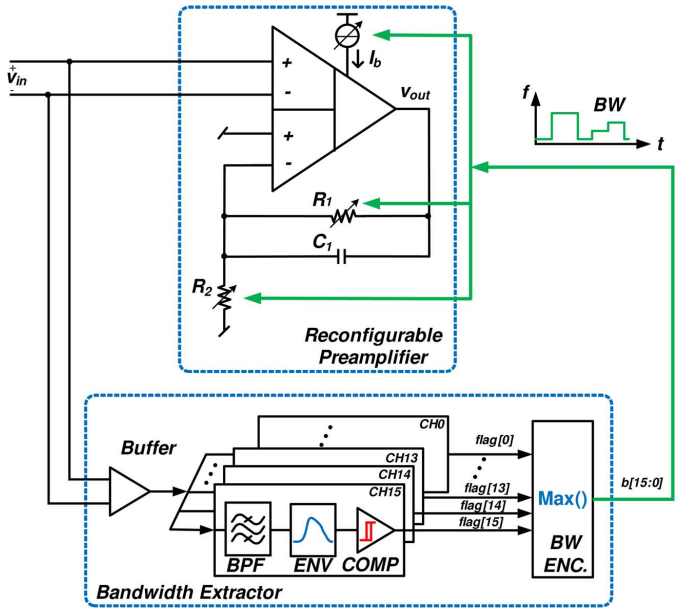


Fig. 2. The system architecture of the bandwidth-adaptive microphone preamplifier. The system consists of a reconfigurable preamplifier and a bandwidth extractor.

$i$'th channel is $\mathrm{flag}[i] \in \{1, 0\}$. This output indicates whether or not the envelope is higher than the threshold that would signify the start of a speech event in this channel [21]. The output of the bandwidth encoder is the index number of the highest frequency channel with a comparator output of $\mathrm{flag}[i] = 1$.

As the bandwidth extractor introduces additional power, an important consideration of our scheme is that the power saved by the bandwidth adaptation should be significantly more than the additional power consumption of the bandwidth extractor. This is realized by the fact that the bandwidth extractor allows much lower dynamic range and hence higher noise level compared to the preamplifier, as shown in Fig. 3.

The amplitude of speech spans a usable dynamic range (UDR) of 40 dB [22], [23]. For humans to perceive speech as "clean", the signal-to-noise ratio (SNR) of the speech needs to be at least 40 dB [23], [24].

A linear time-invariant (LTI) preamplifier would need an input dynamic range of at least 80 dB, in order to ensure a minimum 40-dB SNR across the entire speech UDR [16]. (For input amplitudes on the high end of the UDR, the SNR would be 80 dB; for amplitudes on the low end of the UDR, the SNR would be 40 dB.)

In fact, any preamplifier that does not perform dynamic range compression (our reconfigurable preamplifier, for instance, does not) would need a dynamic range of 80 dB to process perceptually-clean speech.

While our reconfigurable preamplifier must be designed for a dynamic range of at least 80-dB, the bandwidth extractor can be designed with a 40-dB dynamic range. This is because the bandwidth extractor does not need to maintain a 40-dB SNR; the desired output from the bandwidth extractor is not clean speech, but a frequency channel index. As a result, the bandwidth extractor consumes only 3 $\mu$A, compared to the reconfigurable amplifier's 51 $\mu$A.

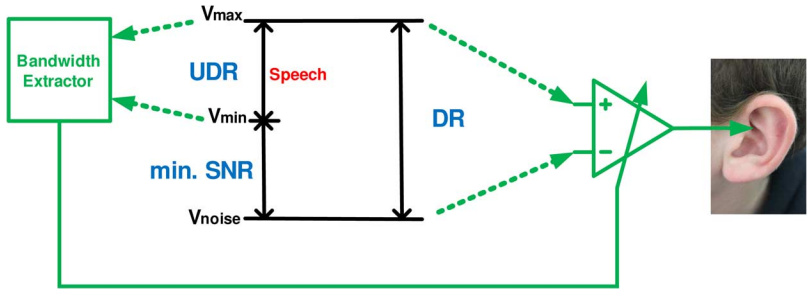


Fig. 3. The different dynamic range requirements for the bandwidth extractor and the preamplifier core. The bandwidth extractor's dynamic range is the speech signal's UDR, as it is only used to detect the speech signal's feature. The preamplifier's dynamic range is the speech signal's UDR plus the SNR needed even for the minimum speech signal to be perceived as clean. The arrows pointing to the bandwidth extractor and the preamplifier core indicate the circuits' noise level and maximum input, instead of the actual input signal's range; for the preamplifier, its input signal's range is still UDR, while it needs a low noise level, leading to high dynamic range.

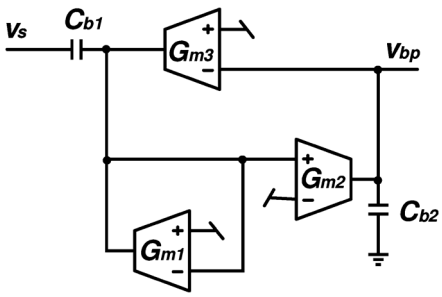


Fig. 4. The bandpass filter in the bandwidth extractor. It is a second-order OTA-C filter, whose center frequency and bandwidth can be programmed by changing the bias current of the OTAs.

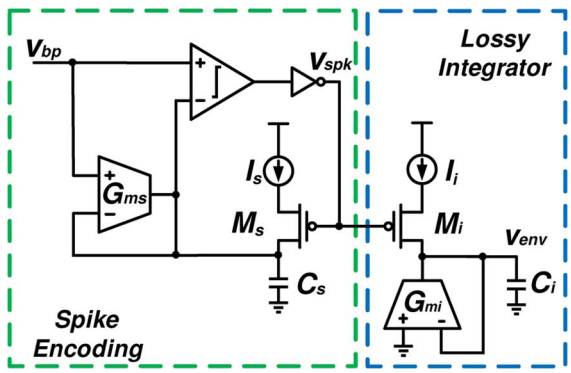


Fig. 5. The envelope detector in the bandwidth extractor, which is implemented by a spike encoding circuit and a lossy integrator.

Each block of the bandwidth extractor is implemented as follows. It should be noted the current consumption given for each building block is the simulated nominal value that is subject to some change due to tuning of the bandwidth extractor's parameters.

### A. Input Buffer

The input buffer is used to drive the bandpass filter bank. It has the same circuit topology as the core preamplifier, whose design details will be discussed in Section IV. However, it has only 40-dB dynamic range. As explained above, the narrow dynamic range is the minimum necessary to process a speech signal and extract its bandwidth, and it relaxes the noise and power requirements of the input buffer. In addition, the buffer has a fixed 4-kHz bandwidth, without reconfigurable capability. The current consumption of this buffer is 1.3 $\mu$A.

### B. Bandpass Filter

Each bandpass filter is a second-order OTA-C filter [25], whose center frequency and bandwidth are both controlled by the OTAs' bias currents, achieving a constant quality factor (Q) with logarithmically-spaced center frequencies, as shown in Fig. 4.

The transfer function of the bandpass filter is:

$$H_b(s) = A_0 \cdot \frac{\frac{\omega_c}{Q}s}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2} \tag{4}$$

where the DC gain $A_0$, center frequency $\omega_c$ and quality factor $Q$ are expressed respectively as below:

$$A_0 = \frac{C_{b1}}{C_{b2}} \cdot \frac{G_{m2}}{G_{m1}}, \tag{5}$$

$$\omega_c = \sqrt{\frac{G_{m2}G_{m3}}{C_{b1}C_{b2}}}, \tag{6}$$

$$Q = \sqrt{\frac{C_{b1}}{C_{b2}} \cdot \frac{G_{m2}G_{m3}}{G_{m1}^2}}. \tag{7}$$

$G_{m1}$, $G_{m2}$ and $G_{m3}$ are all in subthreshold region, so that their transconductance is proportional to their bias current. If we space their bias currents by a fixed ratio and keep the capacitors $C_{b1}$ and $C_{b2}$ constant, we can obtain each $\omega_c$ needed for the 16 bandpass channels with constant $Q$ and $A_0$.

In this design, we set the lowest and highest center frequencies of the 16 bandpass filters to 220 Hz and 3.6 kHz, respectively, with $Q = 5$ and $A_0 = 10$. The total current consumption for all 16 bandpass filter is 0.3 $\mu$A.

Compared to active-RC filters, the OTA-C filter's transfer function can be simply tunable by the bias current. Also, an OTA-C filter may be more area efficient to implement a low-frequency filter with large time constant, compared to an active-RC filter implemented by poly resistors.

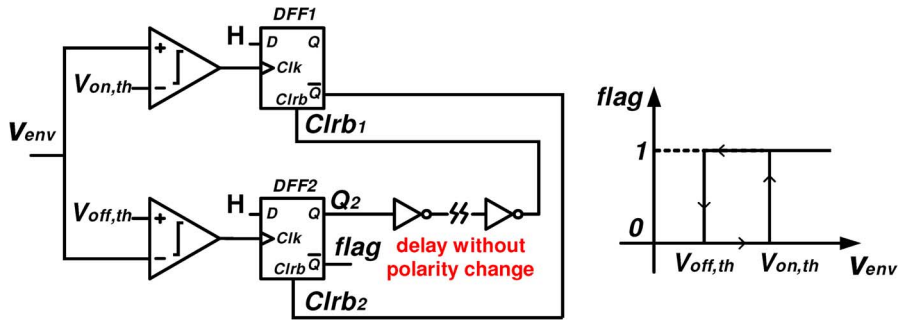


Fig. 6. The hysteretic comparator in the bandwidth extractor, which has easily programmable onset and offset threshold voltages.

### C. Envelope Detector

The envelope detector is implemented with a spike encoding circuit [26], cascaded with a lossy integrator, as shown in Fig. 5. The spike encoding circuit outputs $v_{\rm spk}$, which is an asynchronous train of short pulses whose density represents the envelope of the bandpassed signal, $v_{\rm bp}$. The OTA-C lossy integrator then averages $v_{\rm spk}$ over a window of time. The averaged signal, $v_{\rm env}$, is a measure of the pulse density; the higher the value of $v_{\rm env}$, the more likely that it signifies the start of a speech event.

Discussed in [26], one advantage of using the spike encoding circuit is its adaptive resolution, which automatically provides higher accuracy for smaller envelope signal without directly increasing the power consumption.

The envelope detector has approximately a 10-ms latency mostly due to the time constant of the leaky integrator $(C_i/G_{mi})$, which is also a significant portion of the whole bandwidth extractor's latency. The latency affects the response speed of the bandwidth extractor to changes in bandwidth. This time constant is selected through experimentation, considering the tradeoff between the latency and the smoothness of the extracted envelope.

All the envelope detectors in the 16 channels are identical, and their nominal total current consumption is about 1 $\mu$A.

### D. Hysteretic Comparator

Two special requirements are needed for this hysteretic comparator: First, the hysterestic comparator should be asynchronous (i.e., clockless). This reduces the cost of additional hardware, power and noise from the clock generation and distribution circuits; also, ideally, the hysteretic comparator's hysteresis range (i.e., the value of onset threshold $V_{\rm on,th}$ and offset threshold $V_{\rm off,th}$) should be programmable, in order to easily control the bandwidth extractor's sensitivity. Because of these two special requirements compared to standard hysteretic comparators, a new custom design is needed.

The hysteretic comparator, as shown in Fig. 6, uses two clock-less comparators (i.e., high-gain amplifiers) to compare the signal $v_{\rm env}$ with the onset threshold $V_{\rm on,th}$ and offset threshold $V_{\rm off,th}$ respectively. The two D flip-flops (DFFs) both have the asynchronous control signal $Clrb$, which sets $Q/\overline{Q} = 0/1$ whenever $Clrb = 0$, regardless of the input or clock signals.

We assume, initially, $v_{\rm env}$ is low and $\rm flag = 0$. When $v_{\rm env}$ starts rising and crosses $V_{\rm off,th}$, the clock input of DFF2 will change from 1 to 0. However, it does not change the output of DFF2, because it only responds to the rising edge of its clock input. The DFF's edge-sensitive (rather than level-sensitive) property is important here.

Thus, only when $v_{\rm env} > V_{\rm on,th}$, a rising edge appears on DFF1's clock input, so that $Clrb_2 = 0$ and hence $\rm flag = 1$. It is worth noting that, although the envelope is usually not perfectly smooth, the DFF's edge-sensitive property makes the circuit more robust to the ripples on the envelope that may cross below $V_{\rm on,th}$ temporarily in the rising process. Meanwhile, $Q_2 = 0$ and it is delayed by $\tau_d$ through an inverter chain to make $Clrb_1 = 0$, so that we can reset $Clrb_2 = 1$, in order to release the refreshing capability of DFF2. The delay $\tau_d$ should be longer than the latency from $Clrb$ to $Q/\overline{Q}$.

Because DFF1 only responds to the rising edge of its clock input, $Clrb_2$ is held at 1 even when $v_{\rm env}$ falls below $V_{\rm on,th}$. Only when $v_{\rm env} < V_{\rm off,th}$, a rising edge appears on DFF2's clock input, making $\rm flag = 0$. Again, we utilize the edge-sensitive property of a DFF here to make the circuit respond to the right threshold and also improve its robustness to the ripples on the envelope. The process to generate flag will repeat if another event occurs.

To meet these requirements of clockless operation and programmable onset and offset thresholds, we have designed a comparator based on two DFFs. Alternative implementations may exist that involve other circuit building blocks, like SR latches.

This custom designed hysteretic comparator needs no clock and has easily programmable onset/offset threshold voltages. All the comparators in the 16 channels are identical, and they consume about 0.1-$\mu$A current in total.

### E. Bandwidth Encoder

All 16 comparator outputs $\rm flag[15:0]$ enter the bandwidth encoder, which is implemented with OR gates. The thermometer coded bandwidth $b[i]$ for channel $i$ is expressed as:

$$b[i] = b[i+1] \vee \rm flag[i] \tag{8}$$

where $\rm flag[i]$ is the flag signal of channel $i$ and $\vee$ is the logic OR operation. We set $b[15]$ to $\rm flag[15]$. In this design, $b[0]$ is always set as 1, in order not to fully shut off the reconfigurable preamplifier and avoid aggressive transient settling process. In a design that allowed the reconfigurable preamplifier to be shut off,

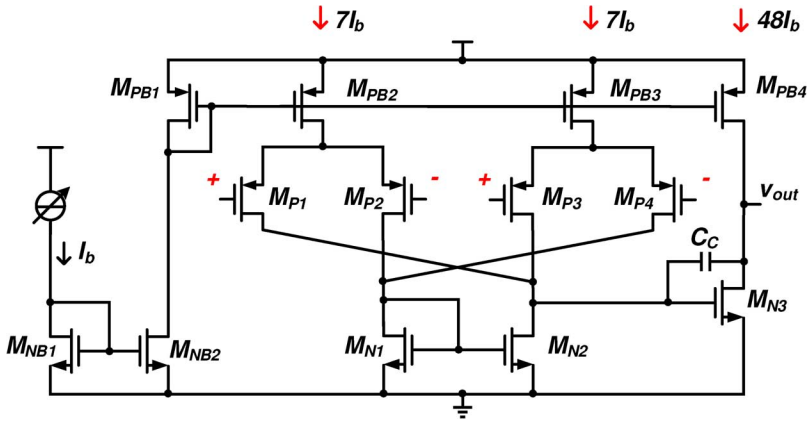


Fig. 7. Schematic of the DDA. It is a two-stage amplifier with double input pairs.

$b[0]$ still would be defined by (8). As we will discuss, the thermometer coded $BW$ naturally matches the thermometer coded $I_b$, $R_f$ and $R_s$ of the reconfigurable preamplifier. The bandwidth encoder's power consumption can be neglected.

## IV. Reconfigurable Preamplifier

The reconfigurable preamplifier is implemented as a differential difference amplifier (DDA) [27] (see Fig. 7) in a non-inverting configuration. A microphone preamplifier usually requires a high input impedance for the condenser microphone to drive [28]. A DDA topology provides a high input impedance and also the option of a balanced input, which has improved robustness to noise and interference coupled from other circuits, particularly in a digital-intensive environment [29]. It should be noted that the balanced input of the DDA is not necessary for this application; it is just an extra feature that would be useful in case it had a differential output signal from the microphone.

In this design, we operate the DDA in the subthreshold region. Although a DDA in the strong-inversion region has a wider linear range, this DDA can still meet the linearity requirement in the subthreshold region, as it has a relatively small input (typically tens of mV) and a relaxed THD specification (<1%).

Taking into account the finite gain and bandwidth of the DDA, the transfer function, $H(s)$, of the reconfigurable amplifier is:

$$H(s) = \frac{1}{\beta}\left(\frac{A_0\beta}{1+A_0\beta}\right)\left(\frac{1}{1+\frac{\tau s}{1+A_0\beta}}\right) \tag{9}$$

where $\beta = R_2/(R_2 + (R_1 \| 1/sC_1))$ and $A_0$ is the DC gain of the DDA. Also, $1/\tau$ is the dominant pole of the DDA. Assuming $A_0 \gg 1$ and $R_1C_1 \gg \tau$, we can write

$$H(s) \approx \underbrace{\left(1+\frac{R_1}{R_2}\right)}_{H_0} \frac{1+sC_1(R_1\|R_2)}{(1+sC_1R_1)\left(1+\frac{\tau s}{A_0}\right)} \tag{10}$$

where we have defined the preamplifier DC gain as $H_0 = (1 + R_1/R_2)$.

As Fig. 8 shows, $H(s)$ has a magnitude transfer function with a low-pass characteristic. Its passband must be wide enough

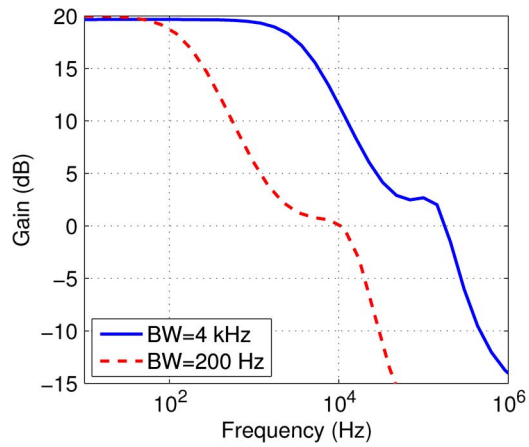


Fig. 8. The simulation results of the transfer function of the reconfigurable preamplifier with bandwidth of 200 Hz and 4 kHz. The rolling-off speed of the transfer function after the zero $z_1$ is faster than 20 dB/decade. This is due to the non-dominant pole in the DDA, which is not taken into account in (10) for simplicity.

to accommodate the bandwidth of the input speech. Since the bandwidth of speech is time-varying, the $H(s)$ passband can also vary in response, in order to save power. We varied $H(s)$ by setting its poles and zeros to be functions of the input speech's bandwidth, $BW$.

The pole and zero due to $R_1$, $R_2$ and $C_1$ are given as:

$$p_1 = \frac{1}{2\pi C_1 R_1} = BW, \tag{11}$$

$$z_1 = \frac{1}{2\pi C_1 (R_1 \| R_2)} = H_0 \cdot BW. \tag{12}$$

To realize these equations, we implemented $R_1$ and $R_2$ each as a resistor DAC, controlled by the output of the bandwidth extractor, as shown in Fig. 9(a).

The second pole of $H(s)$ is $A_0/(2\pi\tau) = g_{m,\mathrm{in}}/(2\pi C_c)$, which is the gain bandwidth product of the DDA ($g_{m,\mathrm{in}}$ is the transconductance of the DDA's input transistors). This pole is chosen to be some large multiple, $G$, of the input bandwidth, and is given as:

$$p_2 = \frac{g_{m,\mathrm{in}}}{2\pi C_c} = G \cdot BW \tag{13}$$

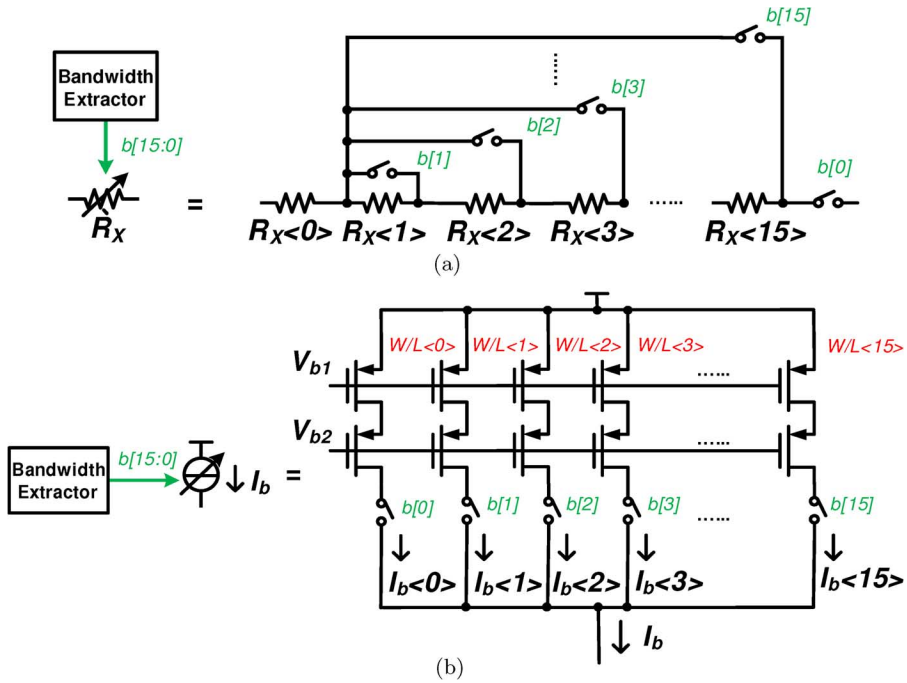


Fig. 9. Thermometer code controlled resistor DAC (a) and bias current DAC (b). The switches are implemented by the transmission gates. In (a), $R_x$ denotes either $R_1$ or $R_2$, as both of them have the same programmable architecture. Because, in this particular design, $b[0]$ is always set as 1, the switch controlled by $b[0]$ is always connected.

The transconductance $g_{m,\text{in}}$ is linearly proportional to the DDA bias current, $I_b$. So, we implemented $I_b$ with a current DAC, which was also controlled by the output of the bandwidth extractor. The bias current DAC is shown in Fig. 9(b), and it produces an output of:

$$I_b = \frac{BW}{BW_{\max}} I_{b,\max} \tag{14}$$

where $BW_{\max} = 4$ kHz is the maximum bandwidth (i.e., the speech bandwidth) and $I_{b,\max}$ is the maximum bias current, corresponding to processing a signal of bandwidth $BW_{\max}$.

In this particular circuit implementation, the DDA's gain bandwidth product $p_2 = g_{m,\text{in}}/C_c$ is about $65 \cdot BW$ $(G = 65)$, where $g_{m,\text{in}}$ can be determined by the bias current of the input stage (see (15)). As we show in the noise and distortion analysis in Section V, the gain bandwidth product corresponds to $I_{b,\max} = 0.79$ $\mu$A and $C_c = 45$ pF.

Also, $C_1 = 112$ pF and $H_0 = 10$, so that the corresponding $R_1$ and $R_2$ can be calculated for any specific $BW$. $C_1$ is chosen considering the tradeoff between capacitor size and the noise: a smaller $C_1$ can save the capacitor size, but it will lead to larger $R_1$ and $R_2$, resulting in degraded noise.

As the reconfigurable preamplifier has 16 bandwidth settings logarithmically ranging from 200 Hz to 4 kHz, the step of bandwidth change is about 22%, which requires relaxed matching performance for the resistor and current DACs. Today's CMOS process can provide device mismatch of better than 1%, and the thermometer-coded DACs have better matching performance compared with the binary-coded DACs.

To sum up, the bandwidth extractor detects the input signal's bandwidth and uses it to control the reconfigurable preamplifier's circuit parameters to implement a bandwidth-adaptive preamplifier with adaptive power consumption. Fig. 10 shows the bandwidth-adaptive preamplifier's power consumption for an input chirp signal [12], where we find the preamplifier's power consumption follows the trend of the frequency change, achieving adaptive power consumption.

## V. Circuit Analysis

As (14) suggests, the power consumption of the preamplifier adapts as a function of the input signal's bandwidth. In this section, we will analyze the effect of this adaptive power consumption on the preamplifier's important performance parameters, including noise, distortion and slew rate.

### A. Noise

If we operate all of the four input transistors of the DDA $(M_{P1} - M_{P4})$ in the subthreshold region, the transconductance $g_{m,\text{in}}$ of each transistor is expressed as:

$$g_{m,\text{in}} = \frac{\kappa\alpha I_b}{V_T} = \frac{\kappa\alpha I_{b,\max}}{BW_{\max} V_T} BW \tag{15}$$

where $I_b$ is the bias current, $\kappa$ is the gate coupling coefficient that is about 0.7, $\alpha$ is the scaling factor from $I_b$ to the transistor's bias current by the current mirrors, and $V_T$ is the thermal voltage $kT/q$ ($q$ is the magnitude of the electrical charge on the electron), which is about 26 mV at room temperature.

The whole preamplifier's thermal noise is primarily determined by its first stage's transconductance $g_{m,\text{in}}$ and $g_{m,\text{c}}$ (the transconductance of the first stage's current mirror load

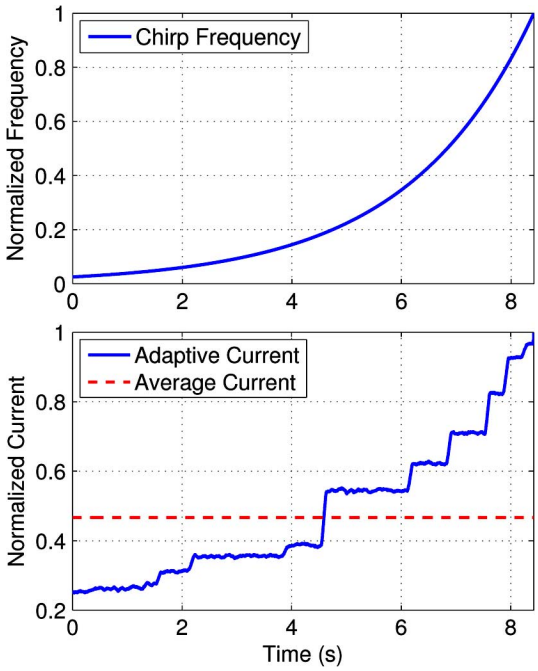


Fig. 10. Measured current consumption (bottom) for an input chirp signal with its frequency sweeping from 100 Hz to 4 kHz logarithmically in 8.4 s (top) in [12]. The current consumption follows the trend of the chirp frequency, and its average is 46.6% of the maximum. Both the frequency and the current consumption are normalized to the maximum value.

$M_{N1}/M_{N2}$), as well as $R_2$, so that the input referred noise power density $v_{n,\mathrm{in}}^2/\Delta f$ of the preamplifier is expressed as:

$$\frac{v_{n,\mathrm{in}}^2}{\Delta f} = 4kT\left(R_2 + \frac{4\gamma}{g_{m,\mathrm{in}}} + \frac{2\gamma g_{m,\mathrm{c}}}{g_{m,\mathrm{in}}^2}\right) = \frac{4kT}{BW}\left[\frac{1}{(H_0-1)2\pi C_1} + \frac{8\gamma BW_{\max} V_T}{\kappa\alpha I_{b,\max}}\right], \quad (16)$$

where $\gamma$ is the noise factor for MOS transistors that is about 2/3. Assuming all the noise is band limited by $BW$, the total input referred noise of the preamplifier is simply:

$$v_{n,\mathrm{in}}^2 = \left(\frac{v_{n,\mathrm{in}}^2}{\Delta f}\right) BW = 4kT\left[\frac{1}{(H_0-1)2\pi C_1} + \frac{8\gamma BW_{\max} V_T}{\kappa\alpha I_{b,\max}}\right], \quad (17)$$

which is constant for any $BW$.

The targeted input referred noise voltage of the preamplifier is 3 $\mu\mathrm{V_{rms}}$. According to (17) and the current mirror factor ($\alpha = 3.5$) shown in Fig. 7, we need $I_{b,\max} = 0.59$ $\mu$A to achieve the required noise level. The simulation results show that the actual needed $I_{b,\max}$ is 0.79 $\mu$A. This discrepancy is due to the second-order effects.

The preamplifier's flicker noise is largely reduced by using large transistor sizes. Furthermore, the input-referred flicker noise voltage density only depends on the CMOS process parameters and the transistor sizes, so that even the residual flicker noise of preamplifier is constant for any $BW$. Therefore, the adaptation does not affect the preamplifier's noise performance.

### B. Harmonic Distortion

Using the method similar to that proposed in [30], we can deduce the expression for the relative third-order harmonic (referred to the fundamental tone) of the system:

$$\mathrm{HD}_3 = \frac{\kappa^2 V_A^2}{24 g_{m,\mathrm{in}}^3 |Z_1|^3 g_{m,2}^3 R_2^3 V_T^2} \quad (18)$$

where $V_A$ is the input sinusoid signal's amplitude, $Z_1$ is the DDA's first stage's output impedance and $g_{m,2}$ is the DDA's second stage's transconductance.

For the in-band frequency, $|Z_1| \approx 1/(2\pi f A_2 C_c) \approx 1/(2\pi BW g_{m,2} R_1 C_c)$, assuming the DDA's first stage's output resistance is large enough to neglect, the DDA's second-stage's gain $A_2 \approx g_{m,2} R_1$ and $BW$ exactly matches the input frequency $f$. Therefore, (18) can be written as:

$$\mathrm{HD}_3 = \frac{\kappa^2\pi^3 BW^3 C_c^3 (H_0-1)^3 V_A^2}{3 g_{m,\mathrm{in}}^3 V_T^2} = \frac{\pi^3 BW_{\max}^3 C_c^3 (H_0-1)^3 V_T V_A^2}{3\kappa\alpha^3 I_{b,\max}^3}. \quad (19)$$

As a result, $\mathrm{HD}_3$ is constant for any $BW$. The third-order harmonic is the prominent harmonic part, so that we can expect that the preamplifier's THD is mostly not corrupted by bandwidth adaptation.

As $I_{b,\max}$ is already chosen according to the noise requirement, the parameter to determine $\mathrm{HD}_3$ is $C_c$. For a maximum input amplitude of 100 mV and the corresponding THD of 1% (the maximum acceptable THD for many audio applications [6], [31]), $C_c$ can be calculated as 106 pF, assuming $\mathrm{HD}_3 \approx \mathrm{THD}$.

The simulation results show that the needed $C_c$ is in fact about 45 pF. The discrepancy between the calculated and simulated values are expected, as the original model proposed in [30] admits an error of several dB. Given the simplicity and reasonable accuracy of the model, it provides us with important intuition to choose initial circuit parameters, which can be refined through simulation.

Although a smaller $C_c$ would lead to better $\mathrm{HD}_3$, it would also make the bias current of the DDA's second stage $I_{b,2}$ higher, in order to maintain enough phase margin.

The phase margin of the preamplifier's feedback loop is 67°, by choosing $I_{b,2} = 48 I_b$. The phase margin keeps constant with the bandwidth adaptation, so that the preamplifier is always stable.

In addition, the preamplifier's slew rate is proportional to $BW$, so that the preamplifier can always provide enough slew rate corresponding to the input bandwidth. Thus, the preamplifier will not generate significant harmonic distortions due to insufficient slew rate.

To sum up, the preamplifier's bandwidth and power consumption are adaptive, so that power efficiency is improved, while the preamplifier's important specifications are not corrupted.

## VI. Circuit Performance Measurement

The microphone preamplifier was fabricated in a 0.5-$\mu$m CMOS process, and operated with a power supply voltage of 2.4 V. Its micrograph is shown in Fig. 11. In order to compare

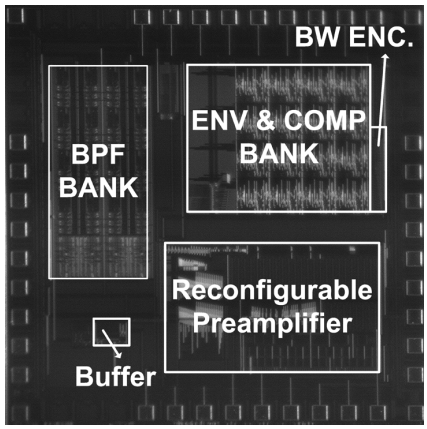


Fig. 11. Die micrograph of the adaptive microphone preamplifier fabricated in a 0.5-$\mu$m CMOS process. The chip die size including the bonding pads is 2.7 mm $\times$ 2.7 mm.

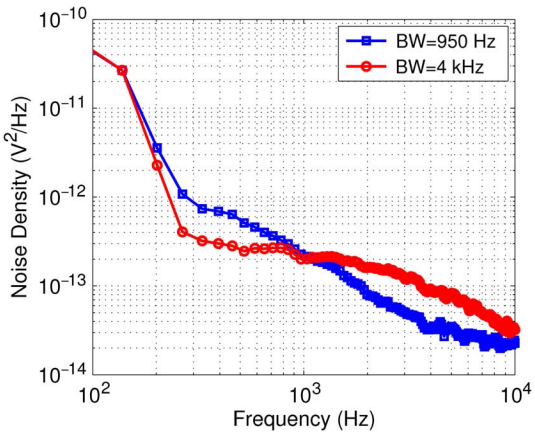


Fig. 12. Measured output noise power density for two preamplifier's bandwidth settings. The flicker noise corner is about 250 Hz.

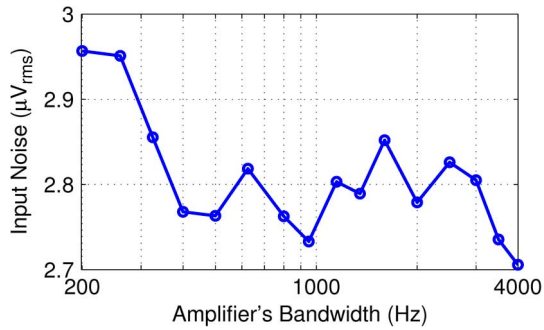


Fig. 13. Measured total equivalent input referred noise voltage and the corresponding preamplifier's bandwidth.

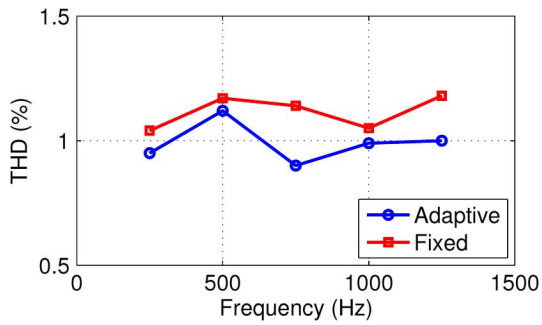


Fig. 14. Measured output THD of the preamplifier with adaptive bandwidth and fixed (4-kHz) bandwidth with 80-$\mathrm{mV_{rms}}$ input sinusoid at different frequencies. The input frequencies are chosen to at least make their third-order hamonics inside the speech bandwidth of 4 kHz.

the adaptive preamplifier's performance with a fixed-bandwidth counterpart of maximum bandwidth, the fixed preamplifier can be realized by forcing the bandwidth code of the preamplifier $b$[15:0] to be all 1.

Fig. 12 shows the output noise power density for two preamplifier's bandwidth settings. We find the noise bandwidth corresponds to the preamplifier's bandwidth, and the *in-band* noise density decreases as the bandwidth increases, so that the total output noise (integrated from 200 Hz to 4 kHz) remains constant. For the two bandwidth settings, the preamplifier's total output noise voltage is 27.4 $\mu\mathrm{V_{rms}}$ and 27.1 $\mu\mathrm{V_{rms}}$, respectively.

Furthermore, we show the total equivalent input referred noise voltage for different bandwidths in Fig. 13. It is less than 3 $\mu\mathrm{V_{rms}}$ and has less than 0.8-dB variance across 20 times of the bandwidth change. The measurement results match our noise analysis in Section V well.

In Fig. 14, the measurement results show that the adaptive preamplifier's output THD keeps reasonably stable with the input frequency, so that the THD is not corrupted by the bandwidth adaptation. We also find that the adaptive preamplifier's THD is always slightly better than that of the fixed preamplifier. It is primarily due to the adaptive preamplifier's bandwidth $(BW)$ is always not greater than the fixed 4 kHz $(BW_{\max})$, so that the harmonics between $BW$ and $BW_{\max}$ will be attenuated by the filtering. The measured input amplitude to generate 1% THD is 112 mV at 1 kHz. This also matches our distortion analysis in Section V, where we predict that the maximum input amplitude is 100 mV, only slightly different from the measurement results.

The bandwidth extraction results for one speech sample are shown in Fig. 15. We can tune the circuit parameters (e.g., the threshold voltages, the spike encoding rate) in the bandwidth extractor to control its sensitivity. For a more aggressive setting, the extracted bandwidth has more active adaptation, more loss of the low-energy speech parts on the time-frequency plane and a lower average current consumption; for a more conservative setting, the extracted bandwidth has weaker adaptation, less loss of the low-energy speech parts and a higher average current consumption. So, there is tradeoff between the current consumption and the retention rate of the speech, which in turn affects the processed speech quality. It is worth noting that the preamplifier has only first-order filtering, so that the low-energy part not covered by the bandwidth in Fig. 15 is not completely removed but just attenuated.

The whole adaptive preamplifier's current consumption is 5–54 $\mu$A, corresponding to its lowest to highest possible bandwidth. The bandwidth extractor's current consumption is less than 3 $\mu$A.

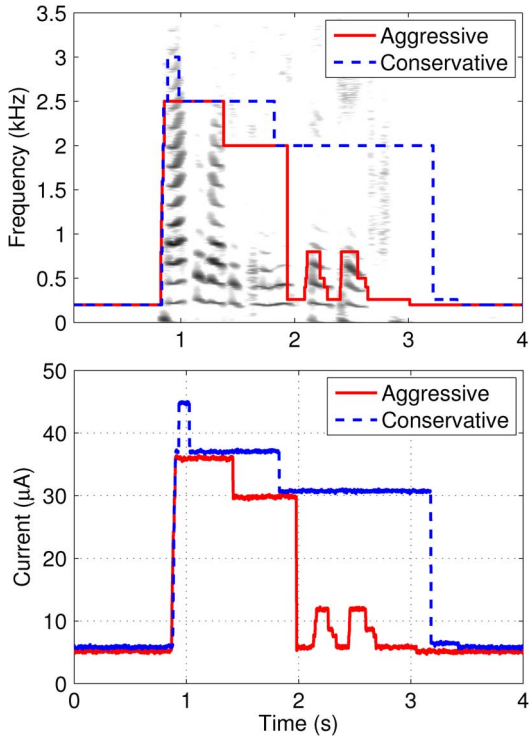


Fig. 15. Measurement results of the extracted bandwidth (top) and the corresponding dynamic current consumption (bottom) for a speech sample with a more aggressive and a more conservative setting, respectively. On the top panel, the speech sample is expressed by its spectrogram that is a time-varying spectral representation of the signal on the time-frequency plane, and the extracted bandwidth are the piecewise lines. The intensity of the darkness on the background indicates the signal's log energy density.

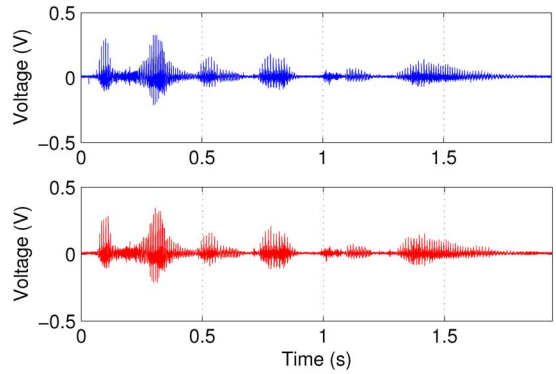


Fig. 16. An example of the measured output signals from the adaptive (top) and the fixed (bottom) preamplifiers. There exists little significant distortion in the output signal from the adaptive preamplifier, compared to that from the fixed preamplifier as the template.

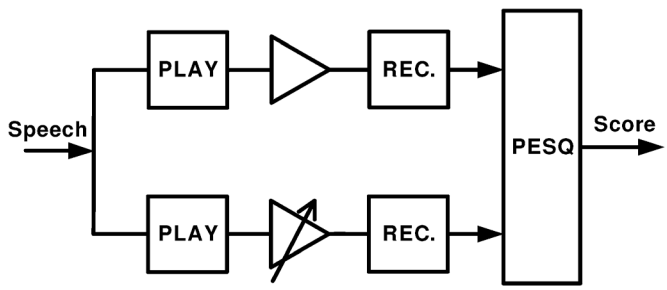


Fig. 17. Test set-up for PESQ measurement. We used the audio codec on the computer sound card with 8-kHz sampling rate and 16-bit resolution to play the original and record the processed speech samples. The upper channel is for the fixed-bandwidth preamplifier, while the lower one is for the adaptive-bandwidth preamplifier. The PESQ algorithm is provided by [36], and we used the American English speech samples provided by [37] in this measurement.

## VII. Speech Quality Assessment

The adaptive amplifier's bandwidth is time varying, so that the performance of the real-time bandwidth detection will affect the signal's quality. Shown in Section VI, the sensitivity settings of the bandwidth extractor directly affect the speech quality. Also, in the bandwidth extractor, the finite number of the frequency channels limits the bandwidth extraction's accuracy, and the latency of the circuits limits the speed. These effects cannot be quantified by dynamic range measurements alone. Although we have shown that there exists little observable discrepancy between the output signals from the adaptive and the fixed preamplifiers in [12] (see Fig. 16), more rigorous assessment is needed. Therefore, we need to directly evaluate the speech quality.

We used the perceptual evaluation of speech quality (PESQ), an industrial standard for objective speech quality assessment [32], to evaluate the quality of speech after it has been processed by the adaptive amplifier. The attraction of PESQ is that it shows a 0.935 correlation to subjective human listening tests of speech quality [32], [33]. PESQ compares processed speech to an "uncorrupted" reference signal, assigning it a score that is calculated as:

$$\mathrm{PESQ} = 4.5 - 0.1D - 0.0309A \tag{20}$$

where $D$ is the average disturbance value that measures the absolute audible error and $A$ is the asymmetric average disturbance value that measures any audible errors that are significantly louder than the [32], [34], [35]. For instance, a global system for mobile (GSM) network in typical operating range has a PESQ score of 3.1 to 3.6, a toll-quality voice codec (G. 728) achieves a PESQ score of 3.8, and a modern integrated services digital network (ISDN) can obtain a PESQ score of 4.3 [35].

The measurement set-up for PESQ with an audio codec is shown in Fig. 17. Audio codecs themselves inevitably affect the speech quality [38], and we measured that the codec itself (not affected by the adaptive preamplifier) in the test set-up can at most achieve a PESQ score of around 4.1. For our reference signal, we used speech processed by a fixed-bandwidth preamplifier (that is, with the reconfigurable amplifier's bandwidth held at a constant 4 kHz).

The adaptive preamplifier's average current consumption is programmable by tuning the bandwidth extractor's sensitivity setting, and we get the corresponding PESQ scores shown in Fig. 18. The PESQ score reaches the maximum achievable value of 4.1 with 27-$\mu$A current consumption, which is 50% of the conventional fixed 4-kHz preamplifier's current consumption. With 84% saving of current consumption, the PESQ score reduces to lower than 3.8, which is still sufficient for toll-quality applications. Therefore, the speech quality is programmable to achieve the requirement for the specific applications and we can obtain corresponding savings in power consumption.

TABLE I
PERFORMANCE COMPARISON

| | This Work | [39]‡ JSSC'12 | [31] ISSCC'09 | [6] JSSC'03 | [40]# JSSC'12 |
|---|---|---|---|---|---|
| $\mathbf{V_{noise(input)}}$ ($\mu V_{rms}$) | 3 | 3.6 | 5§ | 5 | 1.8 |
| $\mathbf{V_{max(input)}}$ ($mV_{rms}$) | 80 | 85 | 67£ | 52 | 56 |
| **THD @ $\mathbf{V_{max(input)}}$** (dBc) | $-40$ | $< -84$ | $-40$ | $-40$ | $-83$ |
| **Gain** (dB) | 20 | 19.5 | 8 | 20 | 22# |
| **DR** (dB) | 89 | 87 | 83 | 80 | 90 |
| $\mathbf{f_{BW}}$ (kHz) | 4 | 20 | 20 | 10 | 4 |
| $\mathbf{I_{tot}}$ ($\mu$A) | $< 27$† | 220$ | 120 | 34 | 350 |
| $\mathbf{V_{dd}}$ (V) | 2.4 | 1.5 | 1.8 | 2.8 | 1.5 |
| **Power** ($\mu$W) | $< 65$† | 330$ | 216 | 96 | 525 |
| **CMOS process** | 0.5-$\mu$m | 40-nm | 0.18-$\mu$m | 1.5-$\mu$m | 0.13-$\mu$m |
| **High Input Impedance** | YES | NO | YES | NO | YES |
| **FoM** (dB) | $> 167$† | 165$ | 163§ | 160 | 159 |
| **NEF** | $< 9.5$† | 14.5$ | 14.9§ | 11.2 | 20.5 |

$$\text{FoM} = \text{DR} + 10\log[(f_{BW}/P)\cdot 1\text{J}] \text{ (Higher FoM means better power efficiency.)}$$

$$\text{NEF} = V_{\text{noise(input)}}\cdot\sqrt{2I_{\text{tot}}/\pi V_T 4kTf_{BW}} \text{ (Lower NEF means better current efficiency.)}$$

† The upper limit of the current/power consumption and NEF, as well as the lower limit of the FoM, correspond to the case without speech quality degradation (when PESQ = 4.1).

‡ This design can achieve higher DR at a special line-in mode with 0-dB gain, mostly due to large input amplitude (1.13 V), which is not the amplitude a typical microphone can provide. So, we choose its specifications for the regular microphone readout mode, the same as all the other designs.

$ This design has a low input impedance and needs a buffer to be driven by a condenser microphone. The buffer's power consumption is not included. If it were included, this design would consume more current/power and have degraded FoM and NEF.

§ The noise is A-weighted. The unweighted noise, FoM and NEF would be worse. For instance, the results in [39] show that the unweighted noise is about 2–4 times of the weighted noise.

£ Based on the input amplitude with 1% THD. Lower input can generate lower THD.

# Although this design has 2.6 dB lower noise at the 42-dB gain mode, the overall DR is 16.4 dB higher at the 22-dB mode, which is therefore selected for comparison.

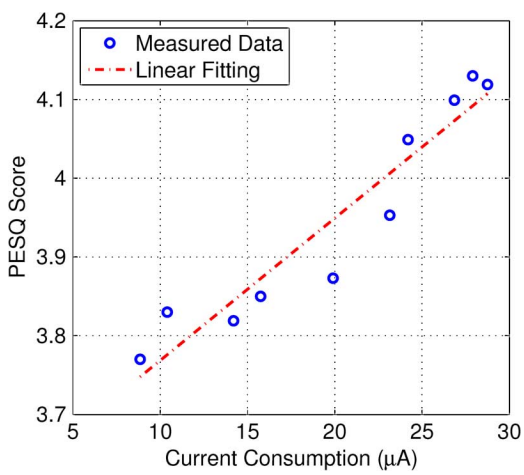


Fig. 18. Measured PESQ scores and the corresponding current consumption. The data is based on the average results of all the speech samples we used.

## VIII. BENCHMARKING

Table I summarizes the performance of the preamplifier and compares it with other low-power microphone preamplifiers.

Following the examples of [39], [40], we define a figure of merit (FoM) for audio preamplifiers as:

$$\text{FoM} = \text{DR} + 10\log\left(\frac{f_{BW}}{P}\cdot 1\text{J}\right) \tag{21}$$

where the "1J" term is used to make the FoM dimensionless.

Noise efficiency factor (NEF) [41] can also be used as another FoM to evaluate the preamplifier's current efficiency in achieving a noise specification at a given bandwidth:

$$\text{NEF} = V_{\text{noise(input)}}\cdot\sqrt{\frac{2I_{\text{tot}}}{\pi V_T 4kTf_{BW}}} \tag{22}$$

where $V_{\text{noise(input)}}$ is the total input referred noise voltage's rms value and $I_{\text{tot}}$ is the total current consumption.

*Higher* FoM indicates *higher power efficiency* for achieving the DR with bandwidth of $f_{BW}$, while *lower* NEF indicates *higher current efficiency* for achieving the noise level with bandwidth of $f_{BW}$.

## IX. Conclusion

We have presented a bandwidth-dependent adaptation method for improving a preamplifier's power efficiency. The bandwidth-adaptive preamplifier significantly reduces its power consumption while maintaining a constant dynamic range. Compared to a conventional preamplifier with fixed bandwidth, our circuit does not degrade speech quality even for 50% power saving. Also, our preamplifier can be programmable to achieve up to 84% power saving with less than 0.4 PESQ score degradation.

As a system-level design strategy, a bandwidth-adaptive circuit provides a new approach for efficiently processing real-world signals that have variable bandwidth. Our results show that such a circuit exhibits adaptive power consumption that corresponds to the input signal's bandwidth, without loss of dynamic range. Beyond dynamic range measurements, we have also studied the tradeoff that our circuit has between power consumption and signal quality (as measured by PESQ).

Applying this bandwidth-adaptive method to an AFE is particularly important in power-constrained sensors, where the AFEs' power consumption often dominates the limited power budget. Therefore, this method could play an important role in enabling or improving many emerging low-power sensor applications.

Finally, we note that the bandwidth-adaptive method and certain amplitude-adaptive methods [16]–[18] belong to the same general class of input-dependent power adaptation schemes. As discussed in [16]–[18], amplitude-adaptive circuits adjust their noise levels—and hence power consumption—according to the input amplitude. An interesting future direction would be to combine both techniques of bandwidth- and amplitude-adaptation in a single system.

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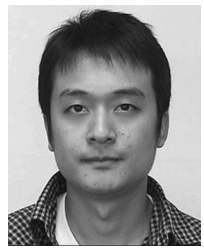

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