A High Frequency Read-Out Channel for Bio-Impedance Measurement

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***Abstract*—In this paper, a high frequency read-out channel for electrical impedance imaging is presented. The channel comprises an instrumentation amplifier (IA), automatic gain control (AGC), high-resolution delta sigma analog-to-digital converter (ADC), mixer, and ADC buffer. Design details of the channel are described, and the performance of the ADC and the entire channel are reported, based on simulation results from a 0.18 μm CMOS technology. The power consumption of the proposed read-out channel is 7.6 mW.**

***Keywords*—impedance imaging, instrumentation amplifier, IA, mixer, buffer, sigma delta, ADC.**

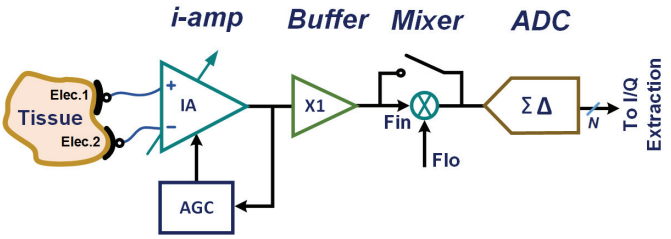

Fig. 1. Simplified block diagram of the read-out channel, including instrumentation amplifier (IA) plus automatic gain control (AGC), buffer, mixer and sigma delta ADC

I. INTRODUCTION

Electrical impedance imaging (EII) is an attractive technology for biomedical imaging, because it is cheap, non-ionizing, and potentially miniaturizable [1]. EII works by injecting a sinusoidal current into the volume of interest and then using the amplitudes and phases of the resulting boundary voltages to extract spectral parameters and also to generate a tomography-like impedance map.

Certain EII applications, like discriminating tissue with high- versus low-grade cancer, require a wide frequency range of operation, from 100 Hz to well over 1 MHz [2]. In addition, because image reconstruction is an ill-posed problem, the EII instrumentation must maintain an SNR of between 80 to 100 dB [3]. An analog-to-digital converter (ADC) that was part of an EII instrumentation read out chain would therefore need to provide at least 14 bits of resolution.

High resolution, wide bandwidth ADCs are not an attractive solution for designing an EII system, because their high power consumption and heat dissipation make them unsuitable for miniaturization. For instance, a state-of-the-art 14-bit, 35 MSa/s ADC consumes over 50 mW of power [4]. To ease the ADC speed (and power) requirements, an alternative approach might involve analog I/Q extraction, as described in [1]. Unfortunately, that solution requires low-noise, precise and highly linear analog components, which again translates to high power consumption [5]. Instrumentation amplifier (IA) as the analog front-end of the EII system also needs to operate over a wide range of frequency, while having a dynamic range of over 80 dB [3]. In this paper a high frequency read-out channel is presented that achieves the high resolution and high dynamic range requirements of EII over a 6 MHz bandwidth, while consuming 7.6 mW of power.

II. OVERVIEW OF PROPOSED SOLUTION

Fig. 1 shows our proposed solution that comprises an instrumentation amplifier, automatic gain control (AGC), buffer, mixer, and ADC as an EII read-out chain. The boundary voltages on the tissue are measured by a set of electrodes and amplified by the IA. The gain of the IA is variable and controlled by the AGC unit, in order to increase the dynamic range of the system. The output of the IA travels through the buffer and either passes through the mixer or bypasses the mixer to reach the ADC. For input signals of 100 kHz or less, the ADC directly converts the boundary voltage to a digital output. For frequencies higher than 100 kHz, the mixer first down-converts the boundary voltage to an intermediate frequency (approximately 100 kHz). The ADC then processes this down-converted voltage to produce a digital output. Since the ADC only ever processes signals of 100 kHz or less, it is able to maintain a low power consumption. The mixer is implemented with switches, and is therefore highly linear. Finally, the digital matched filtering that is performed on the ADC output allows for precise amplitude and phase extraction.

III. SYSTEM DESIGN

This section describes the design procedure of the main building blocks of the proposed read-out channel, including the ADC, mixer, and IA.

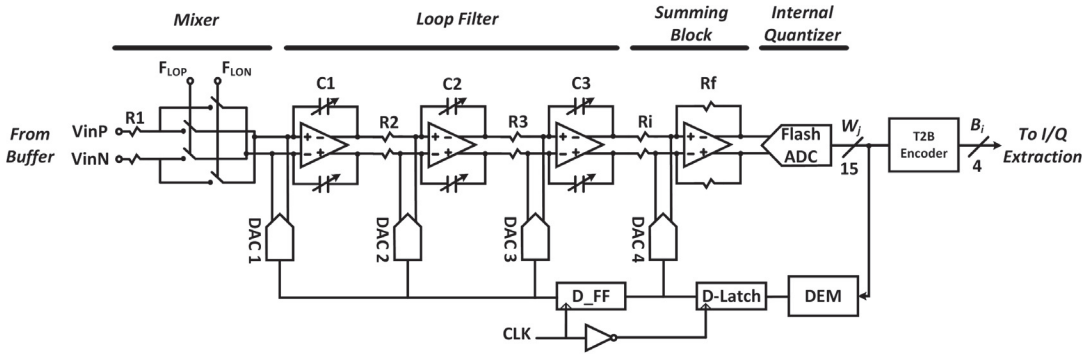

Fig. 2. Continuous-time sigma delta ADC architecture with an upfront passive mixer

A. Continuous-time Sigma Delta ADC

The architecture of the ADC used in this system is shown in Fig. 2. It is a 3rd order, low-pass continuous-time sigma delta ADC with 16 bits of resolution, and sampling rate of 12.8 MHz. The modulator was implemented as a continuous-time converter largely to keep power consumption low; the opamps used in a continuous-time sigma delta ADC require much lower gain bandwidth compared to their discrete-time counterparts [6]. In addition, there is a low-pass filter inherent in the continuous-time sigma delta ADC structure, precluding the need for an explicit anti-aliasing filter [6]. Therefore, the loop filter of the sigma delta modulator acts as an anti aliasing filter as well.

1) Loop filter: In order to implement the loop filter, a cascade-of-integrator-feed-back (CIFB) structure was chosen. An integrator feed-forward (CIFF) structure would have consumed less power, but it also would have introduced zeros in the signal transfer function, causing peaking and instability in the presence of large out-of-band signals. In contrast, the feed-back structure that we chose exhibits a flat signal transfer function. This allows it to remain stable, even when processing the sum frequency signals that are produced by the mixer.

2) Internal Quantizer: Continuous-time sigma delta ADCs are prone to increased noise due to clock jitter. Since the noise induced by jitter is directly proportional to the area under each digital-to-analog converter (DAC) pulse output, employing a multi-bit quantizer and DAC can significantly alleviate this problem [7]. Therefore, we implemented the modulator's internal quantizer as a 4-bit flash ADC, which comprises a resistor ladder, 15 charge distribution comparators, and a thermometer-to-binary converter.

3) Operational Amplifiers: The operational amplifier (op-amp) in the first integrator must sink/source a wide range of currents. To efficiently meet this requirement, this op-amp was implemented with the class AB structure shown in Fig. 3 (a) [8]. The op-amp used in the 2nd and 3rd integrators, as well as in the summation block, was a traditional two stage amplifier.

4) DACs: The ADC's feedback DACs were implemented as current-steering DACs, as shown in Fig. 4. The first three of these DACs are the main DACs in the modulator feedback loop. The fourth DAC is used along with a clock delay block to accommodate the ADC's non-zero response delay, which can otherwise cause instability in the modulator [9]. Among all these DACs, the first one requires the highest precision, equal to the precision of the entire ADC. The reason is that the output of the first DAC is directly added to the input signal without the benefit of noise shaping. Therefore, any nonlinearity in this DAC can degrade the performance of the ADC. Dynamic element matching (DEM) [10] was used to attain 16 bits precision in the DAC, despite using current sources with only 8-bit matching.

The output current of each DAC is defined based on the coefficients required to implement the loop filter. However, the minimum output current of the first DAC is limited by noise considerations. In order to minimize clock feed-through and the glitch energy caused by switches in the current steering DAC, low-swing high-crossing signal generators [11] were employed to drive the current switches.

5) Programmable Capacitors: Nonidealities during the fabrication process will cause mismatch in the values of the inte-

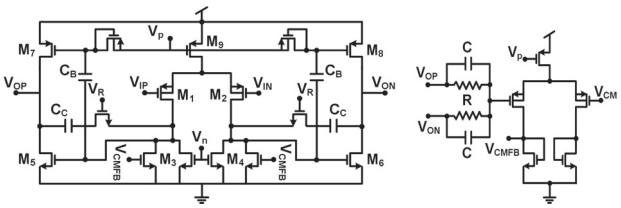

Fig. 3. a) Schematic of the class AB amplifier, and b) resistor averaging common mode feedback (CMFB)

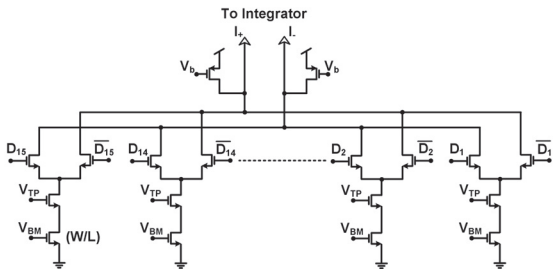

Fig. 4. Current steering DAC schematic

grating resistors and capacitors. Variation of the RC products from their nominal values can degrade the performance of the ADC, and consequently the whole channel. To compensate for these variations, the integrating capacitors were implemented as programmable capacitor bank, allowing the RC values to be trimmed so that the integrator gains remained within an acceptable range.

B. Mixer

A passive switching mixer was employed, as depicted in the left-hand side of Fig. 2. Since the mixer's terminals are connected to the virtual ground nodes of the 1st op-amp's inputs, it is able to achieve high linearity. Input signals of frequency > 100 kHz are mixed down to an intermediate frequency (IF) before being digitized by the ADC. The intermediate frequency is approximately 100 kHz; a higher IF would require a faster, higher power ADC, and a lower IF would degrade the frame rate of the EII system as a whole.

C. Instrumentation Amplifier

The instrumentation amplifier, along with the automatic gain control unit, that precedes the mixer in the read-out chain of Fig. 1 is the same circuit that we previously introduced in [12]. Fig. 5 shows the core of the IA, which is based on the universal current conveyor IA structure. The IA comprises a transconductance stage followed by a transimpedance stage. The differential voltage gain of the IA is set by the ratio of resistors, R_2/R_1. Absolute values of these two resistors will be the dominant factors in determining the bandwidth, noise, and power consumption of the IA.

In order to maintain the frame rate of the imaging system, the gain setting of the IA is required to be determined within a fraction of a period of the input signal. Therefore, the IA utilizes a fast amplitude detection approach [12]. The output of the fast amplitude detection block is used to vary the ratio of R_2 and R_1, in order to achieve different gains of the IA. The gain of the IA would be automatically selected at 0.5, 19 and 38 dB, depending on the amplitude of the input signal. The IA has a dynamic range of 85 dB over a 10 MHz bandwidth, and the current consumption of the core of the IA and AGC are respectively $945\ \mu A$ and $25\ \mu A$ from a 3.3 V power supply, resulting in 3.1 mW of power.

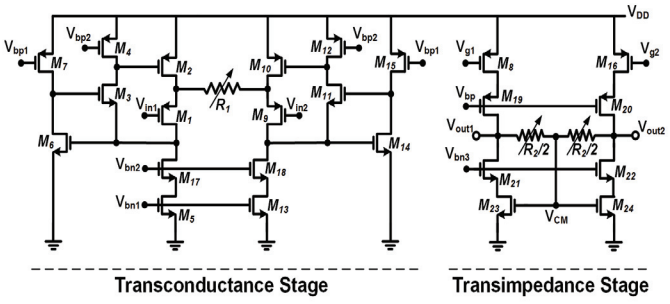

Fig. 5. Circuit schematic of the instrumentation amplifier core

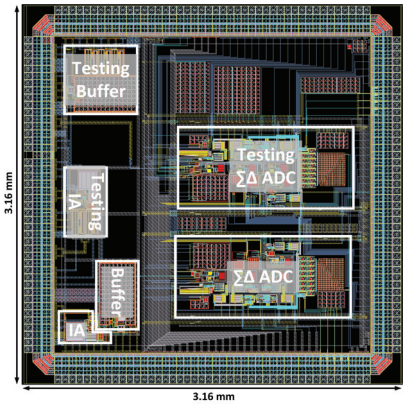

Fig. 6. Layout of the chip including full read-out channel and testing structures

IV. RESULTS

A read-out channel for electrical impedance imaging, including an IA, automatic gain control, buffer, mixer and a 16-bit sigma delta ADC was designed, laid out and simulated in 0.18 μm CMOS technology. The layout of the channel is shown in Fig. 6, which includes a complete channel separately, and also different blocks laid out individually for testing purposes. The area of the chip including pad frame is $10\ mm^2$. The whole channel was implemented as a fully-differential system and has a power consumption of 7.6 mW.

The simulated output spectrum of the stand-alone sigma delta ADC, with 50 kHz input signal shows SNR of 90 dB, as shown in Fig. 7. In order to show performance of the proposed read-out channel, simulations were performed to extract both amplitude and phase of the input signal. In the first test, phase of the input signal was kept constant while input amplitude was swept for different input frequencies, as shown in Fig. 8. In this test, two different frequencies were chosen as an example, in the 1kHz plot the mixer is off and the ADC buffer output will directly pass through the ADC. However, for the 6 MHz input signal, the mixer down converts the signal to an intermediate frequency approximately 100 kHz. For the 2nd test, the input amplitude was kept constant while input phase was swept from 0 to 90 degrees, with steps of 5 degrees, and results are shown in Fig. 9. In this test also for 1 kHz signal mixer is off, while for the 1 MHz signal the mixer performs down conversion.

The power spectrums of the read-out channel for two input

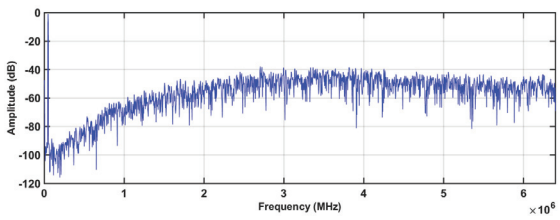

Fig. 7. ADC output spectrum

frequencies of 94.5 kHz and 5.95 MHz are shown in Fig. 10. In Fig. 10 (a), the mixer is off for the 94.5 kHz signal, whereas for the 5.95 MHz input frequency in Fig.10 (b), the mixer down converts the signal to an IF frequency equal to 92.6 kHz. As it can be seen, the matched filter performs as a narrow band filter around the input frequency, which can significantly reduce the out-of-band noise and distortions.

V. CONCLUSION

We have presented a read-out chain for high frequency electrical impedance imaging. The instrumentation amplifier with a fast automatic gain control block achieves a dynamic range of 85 dB. The ADC uses a mixer and sigma delta modulator to cover a wide range of input frequencies up to 6 MHz. The ADC and IA have SNR of 90 dB and 72 dB respectively and consume total power of 7.6 mW. Simulations of the entire read-out chain (including a digital matched filter) show that the proposed chain is suitable for performing phase-sensitive voltage measurements.

ACKNOWLEDGMENT

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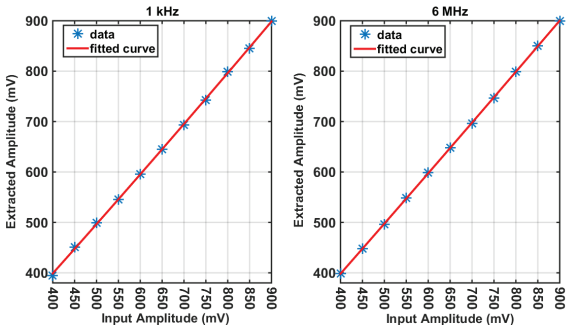


Fig. 8. Input amplitude vs. extracted amplitude for a 1 kHz and 6 MHz input signal

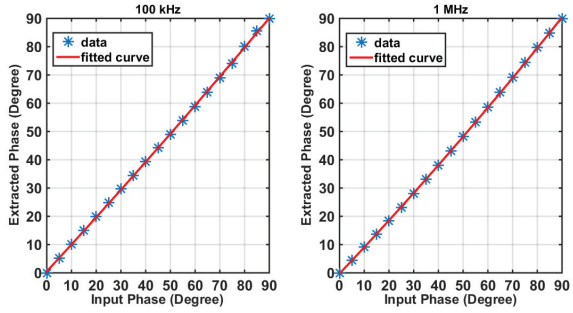
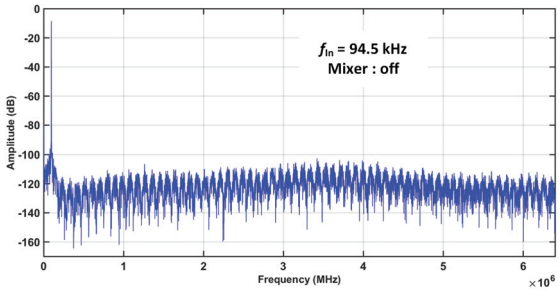
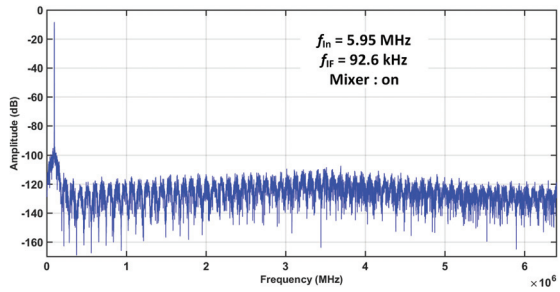


Fig. 9. Input phase vs. extracted phase for a 100 kHz and 1 MHz input signal



(a)



(b)

Fig. 10. Full read-out channel output spectrum after being passed through the matched filter for input frequencies of a) 94.5 kHz, while the mixer is off, and b) 5.95 MHz, while the mixer downconverts the signal to an intermediate frequency equal to 92.6 kHz

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