Analog Integr Circ Sig Process (2014) 81:241–252
DOI 10.1007/s10470-014-0383-0

A microphone readout interface with 74-dB SNDR

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Received: 14 June 2014 / Accepted: 29 July 2014 / Published online: 10 August 2014

Abstract A continuous-time (CT) sigma-delta modulator (SDM) for condenser microphone readout interfaces is presented in this paper. The CT SDM can accommodate a single-ended input and has high input impedance, so that it can be directly driven by a single-ended condenser microphone. A current-sensing boosted OTA-C integrator with capacitive feedforward compensation is employed in the CT SDM to achieve high input impedance and high linearity with low power consumption. Fabricated in a 0.35-μm complementary metal-oxide-semiconductor (CMOS) process, a circuit prototype of the CT SDM achieves a peak signal-to-noise-and-distortion ratio of 74.2 dB, with 10-kHz bandwidth and 801-μW power consumption.

Keywords Continuous-time sigma-delta modulators · Microphone readout · Single-ended to differential conversion · OTA-C integrators · Feedforward compensation

1 Introduction

Currently, many electronic systems have become inherently noisy, mostly due to extensively used digital signal processing. Unlike digital signals, which have high noise margin, analog signals are sensitive to noise and interference. Therefore, a weak output analog signal from a conventional analog microphone (for instance, an electret microphone with a junction field effect transistor (JFET) buffer) can easily be corrupted by noise and interference in a digital-intensive environment (e.g., a circuit board with digital blocks). As a result, incorporating analog-to-digital conversion into microphones leads to a digital output that is more robust to the noisy environment.

A digital microphone needs a readout interface to convert the microphone's output to a digital code for further processing, as shown in Fig. 1(a). The readout interface chip can be packaged in an electret microphone capsule or integrated on the same chip with a micro-electro-mechanical-system (MEMS) microphone, where the microphone's weak analog output signal directly enters the readout interface, so that the microphone capsule will have a digital output externally [1–5].

A common way to implement such a readout interface is using a front-end preamplifier followed by a discrete-time (DT) sigma-delta modulator (SDM) [6, 7]. An alternative approach that is possibly more power-efficient is a continuous-time (CT) SDM that directly senses the microphone's output, which has been used in the previously proposed electret microphone readout interfaces [1, 2]. This approach has inherent anti-aliasing filtering and is usually less power consumptive than its DT counterpart [8]. Such a CT-SDM based readout interface, along with the microphone's simplified circuit model, is shown in Fig. 1(b).

The challenge of interfacing with a condenser microphone is that it typically has a single-ended output, so that, even with a fully-differential topology, the CT SDM based microphone readout usually has considerable even order harmonics [2]. So, previously-proposed CT SDM-based readout circuits produced only a limited effective number of bits (ENOB) due to harmonic distortion [1, 2].

Another issue is that the CT SDM must present a high input impedance in order to be driven directly by the microphone. While many of today's standard CT SDMs

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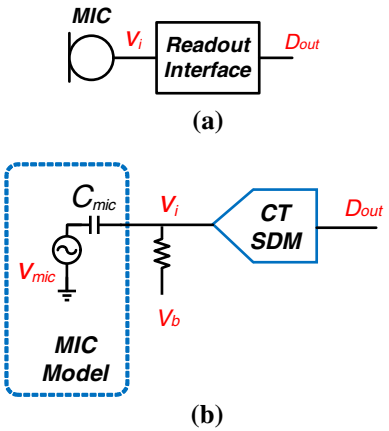

Fig. 1 A digital microphone (**a**) and its circuit model with the readout interface that is implemented by a CT SDM (**b**). The microphone is simply modeled as a voltage source is series with a capacitor. A large resistor is needed to provide the CT SDM with a bias voltage, which can be implemented as a pair of anti-parrallel diode [6, 7]. The resistor is not included in this design

[9–11] exhibit high linearity, their low input impedance makes them unsuitable for microphone readout applications.

In this paper, we present a readout interface based on a CT SDM that can be driven directly by a single-ended condenser microphone. Our CT SDM uses a *current-sensing boosted (CSB) OTA-C integrator* as its first integrator to achieve high linearity as well as high input impedance.

The rest of the paper is organized as follows: the system architecture and specifications of the CT SDM are shown in Sect. 2. In Sect. 3, we discuss the previous integrator topologies with high input impedance and high linearity, and then propose our solution. In Sect. 4, we present the circuit implementation of each building block in the CT SDM. In Sect. 5, we show the measurement results based on a prototype in a 0.35-μm complementary metal-oxide-semiconductor (CMOS) process. Finally, we summarize the paper in Sect. 7.

2 Requirements on microphone readout interface

An audio system (e.g., a digital microphone readout interface) normally needs over 12-bit resolution. The ENOB of a data conversion system is defined as:

$$\text{ENOB} = \frac{\text{Peak SNDR} - 1.76}{6.02}, \tag{1}$$

so that an ENOB of over 12 needs peak signal-to-noise-and-distortion ratio (SNDR) of over 74 dB. Thus, in-band harmonic distortion of the microphone readout interface cannot exceed −74 dBc. In fact, considering the existence of noise, the distortion should be even lower than that to obtain 74-dB SNDR.

The peak SNDR of a microphone readout circuit should be preferably achieved with the microphone's maximum output voltage. Following the discussion in [12], today's condenser microphones (including electret and MEMS microphones) typically have sensitivity in the range of −50 to −38 dBV/Pa [3–5, 13], so that the maximum output voltage that a microphone can provide is between 63 mV_{rms} to 250 mV_{rms} [12]. For instance, the CT SDM proposed in this paper achieves its peak SNDR with 128-mV_{rms} (or 362-mV peak-to-peak) input amplitude (see Sect. 6), which falls into the typical range of a microphone's maximum output amplitude and corresponds to microphone sensitivity of −44 dBV/Pa. Achieving low harmonic distortion (e.g., <−74 dBc) with relatively high input amplitude (e.g., 128-mV_{rms}) is challenging, particularly considering the input voltage is single ended. Even though the circuit topology is fully diffrential, such a single-ended input may lead to considerable even-order harmonics [2].

Some of previously proposed microphone readout circuits can achieve high SNR (more than 75 or even 80 dB), but the harmonic distortion is relatively high, which limits their SNDR to around 60 dB, corresponding to an ENOB of about 10 [1, 2, 7]. Although many audio applications could allow higher distortion compared to more strict requirement on low noise, high-performance audio systems still prefer low distortion and therefore high SNDR [8, 12]. On the other hand, although one microphone readout interface in [6] exhibits an SNDR of 78 dB with the cost of 6-mW power, the power consumption needs to be greatly reduced for low-power systems. Therefore, due to low SNDR or high power consumption of the previous designs, we propose our solution to a high-SNDR and low-power microphone readout interface in this paper.

Also, a microphone readout circuit needs to provide high input impedance, because a condenser microphone has limited driving capability. A condenser microphone may be simply modeled as a voltage source v_m in series with a capacitor C_m, which is typically several pF, while can also be as high as tens of pF. Usually, input resistance R_i of the readout interface needs to be in the order of hundreds of MΩ to several GΩ [4–6], to make the highpass filter corner due to R_i and C_m low enough to avoid attenuating in-band audio signals. As a result, the readout interface that directly connects to the microphone usually has a gate input, and a very large resistor is used to provide bias point for the interface.

Furthermore, input capacitance C_i of the readout interface should also be small enough in order not to attenuate the signal very much by the capacitive voltage divider. The

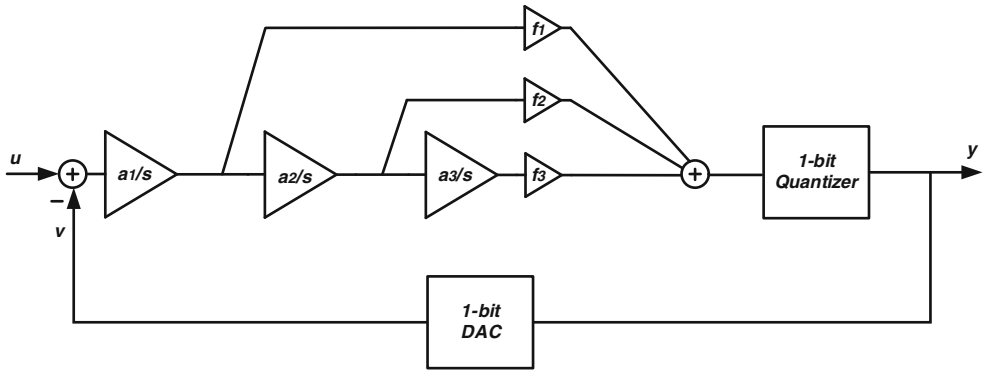

Fig. 2 The system architecture of the third order, 1-bit, feedforward CT SDM

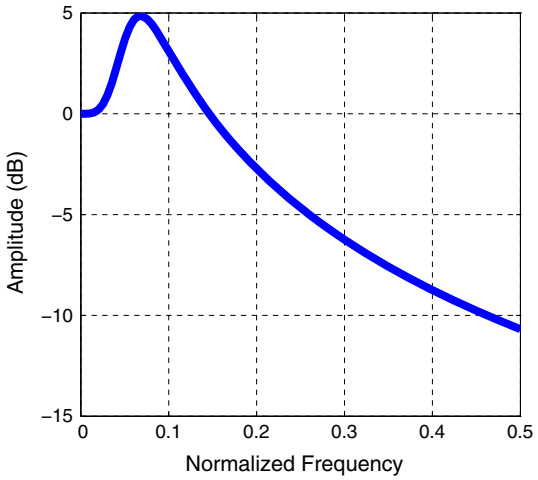

Fig. 3 The CT SDM's simulated STF based on behavior model. The frequency is normalized to the sampling clock frequency

signal voltage enters the readout interface can be expressed as:

$$v_i = \frac{C_m}{C_m + C_i} \cdot v_m. \tag{2}$$

So, the requirement of "high input impedance" is not only applied to DC but also AC impedance.

The input capacitance of the microphone readout interface is typically designed as 2–3 pF [4, 5]. In this design, the equivalent input capacitance of the microphone readout interface is about 1.7 pF. For a typical 5-pF C_m, we have $v_i = 0.75v_m$ according to (2), which introduces about 2.5-dB sensitivity loss. Although reducing the input transistors' size will produce lower input capacitance, it may increase mismatch, flicker noise and also current consumption (to achieve a required transconductance, a smaller transistor size usually needs more current).

In addition, the microphone readout in this specific design has a 10-kHz signal bandwidth, mostly targeted for hearing aid or cochlear implant systems, while the design strategy may be applied to other specific audio applications that require different bandwidth (e.g., 4 or 20 kHz) by changing circuit parameters.

3 System architecture

The CT SDM's block diagram is shown in Fig. 2. It is a third order, 1-bit SDM with feedforward architecture, and the oversampling ratio (OSR) of the SDM is 128. For the audio signal bandwidth of 10 kHz, the sampling clock frequency is accordingly 2.56 MHz. Other combinations of the loop parameters, such as 4-th order, 1-bit and OSR = 64, may also be used to achieve similar performance [1, 2].

Compared to the feedback architecture, the feedforward architecture used in the CT SDM has smaller signal swings at the output nodes of the integrators, resulting in better linearity [14]. An 1-bit quantizer is inherently linear, so that the SDM's linearity is usually higher than the multi-bit loop, although the multi-bit loop can achieve the same resolution with lower OSR or lower order.

The feedforward architecture leads to a peak in the signal transfer function (STF), as shown in Fig. 3, but this peak is far away from the audio band of 10 kHz (or 0.004 normalized to the sampling frequency). The STF has less than 0.001-dB variation in the signal band.

The CT SDM with more details of its building blocks is shown in Fig. 4. The first integrator is a specially-designed CSB OTA-C integrator that will be described in detail in the following sections. The CSB OTA-C integrator will provide a high input impedance and also high linearity even with a single-ended input. The second and third integrators are the conventional active-RC integrators [9–11].

A return-to-zero (RZ) feedback digital-to-analog converter (DAC) is used to alleviate the memory effect in the

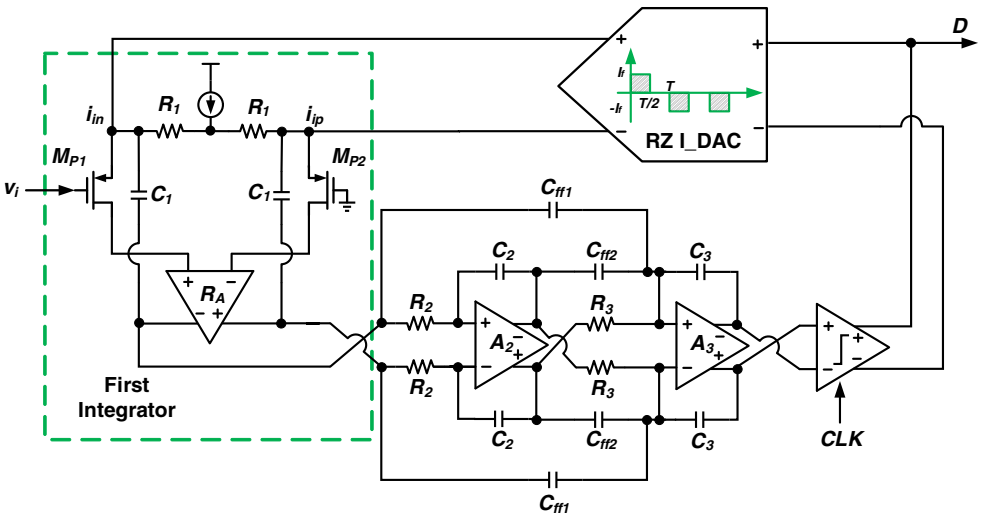

Fig. 4 The CT SDM based microphone readout circuit's building blocks. The loop filter is third order, with the first CSB OTA-C integrator and second/third active-RC integrators. The 1-bit quantizer is a comparator. The feedback DAC is a current-steering RZ DAC

Table 1 Device parameters in CT SDM

R_1 (kΩ)	20
R_2 (kΩ)	400
R_3 (kΩ)	1000
C_1 (pF)	15
C_2 (pF)	1.8
C_3 (pF)	1.2
C_{ff1} (pF)	3.2
C_{ff2} (pF)	2.0
I_{fb} (μA)	18

non-return-to-zero (NRZ) DAC, which would otherwise degrade the CT SDM's linearity by introducing "pattern-dependent" feedback [15].

The summation in the feedforward architecture is implemented by the chain of integrators with weighted capacitive feedforward (CICFF) topology [16], which embeds the summation into the last integrator in the loop filter.

The devices' parameters in the CT SDM can be found in Table 1, where I_{fb} is the value of the feedback current from the NRZ DAC. It is worth noting that the first integrator has much smaller resistor (R_1) and much higher capacitor (C_1), as compared to the second and third stages, in order to reduce the thermal noise, which is primarily determined by the first stage.

4 Integrator topologies with high input impedance and high linearity

The linearity of the first integrator in the SDM is crucial, because it performs the single-ended-to-differential conversion between the microphone and the readout interface. Also, in order to be driven directly by the microphone, the

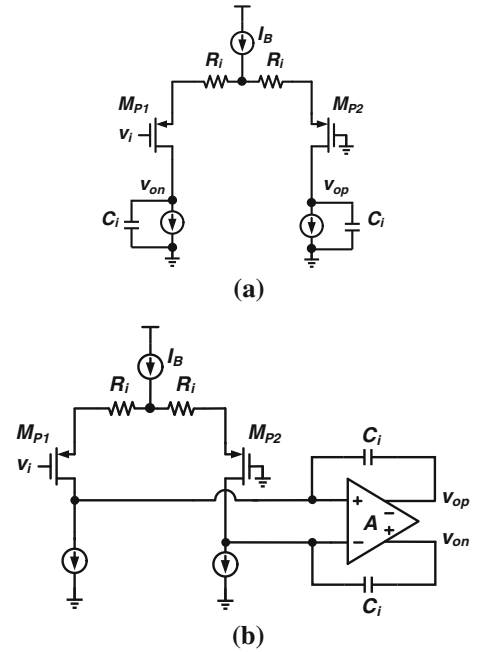

Fig. 5 The OTA-C integrator (**a**) and active OTA-C integrator (**b**). The source-degeneration technique is employed for both integrators

first integrator must have high input impedance. In a conventional CT SDM, the first integrator is typically implemented as an active RC filter to achieve high linearity, but this results in low input impedance [9–11].

In this section, we review two previous OTA-C integrators that have high linearity and high input impedance. We highlight the shortcomings of these previous implementations, and describe how our OTA-C integrator overcomes them.

It should be noted that, in the following discussions, we assume that the microphone readout interface's DC bias voltage V_b is 0 (i.e., connected to the substrate) [2], which

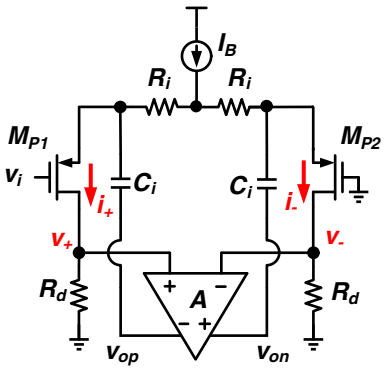

Fig. 6 The VSB OTA-C integrator. The OPA ("A") minimizes $v_+ - v_-$ by the negative feedback, so that $i_+ - i_-$ is also minimized to achieve high linearity

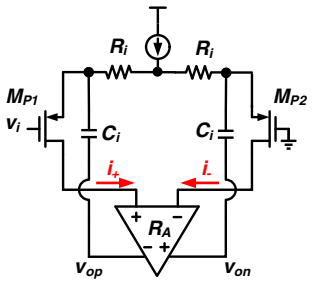

Fig. 7 The CSB OTA-C integrator. The current-to-voltage converter ("R_A") minimizes $i_+ - i_-$ directly by the negative feedback to achieve high linearity

can be very clean. If it was connected to a DC voltage that is generated on chip, the noise and interference in the mixed-signal chip may couple to the input, corrupting the microphone readout system's performance.

4.1 Active OTA-C integrator

As shown in Fig. 5(a), an OTA-C integrator provides high input impedance, as its input is connected to the gates of the transistors. Source degenerated techniques are usually applied to the OTA to improve linearity, and the source-degenerated OTA-C integrator's linearity is determined by $g_m R_i$ (g_m is the transconductance of M_{P1}/M_{P2}): the higher $g_m R_i$ is, the better linearity is. If $g_m R_i$ is large enough, the transconductance of the OTA is approximately $1/R_i$, so that the integrator's transfer function is $H(s) = 1/sR_iC_i$.

The finite and nonlinear output impedance of the OTA will affect the OTA-C integrator's DC gain and linearity. As shown in Fig. 5(b), these non-ideal effects can be mitigated by using an active OTA-C solution [1]. The high-gain operational amplifier (OPA) with negative feedback

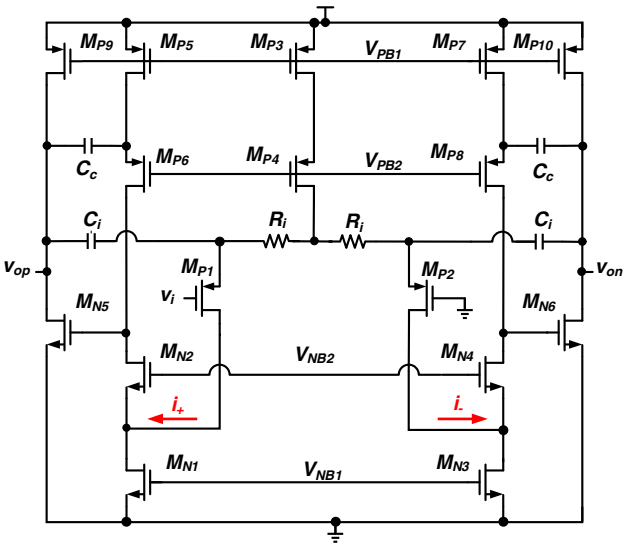

Fig. 8 The CSB OTA-C integrator implemented by a folded cascode stage, as the source of M_{N2}/M_{N4} has low input impedance

provides a very low load impedance to the OTA, on the order of $1/(sC_iA)$. Thus, most of the the OTA output current flows into the capacitor, C_i, and the effect of the finite and nonlinear output impedance of the OTA is reduced.

Although the OPA alleviates the problems of finite DC gain and parasitic nonlinear devices, it cannot help improve the linearity of the source degeneration stage in the OTA. The linearity of the whole integrator will still be limited by the source degeneration stage even if the OPA's gain is infinite. As a result, we still need to increase $g_m R_i$ for better linearity. Because R_i is directly related to the integrator's thermal noise, it cannot be increased aggressively, while increasing g_m leads to more power consumption[1].

In the active OTA-C integrator, the OPA's gain A cannot be utilized to improve the linearity of the source degeneration stage. Instead, the power and hardware cost of a high-gain OPA is only used to alleviate such second-order, non-ideal effects of the OTA. Even though much power is dissipated to make A very high, the linearity of the integrator is still limited by the source degeneration stage. If we can find a way to embed the OPA into the OTA structure and utilize its high gain to improve the source degeneration stage's linearity, we may get better linearity with similar power and hardware cost.

[1] g_m can also be increased by increasing the transistor's size. However, this increase is limited if the transistor is already in the subthreshold region. Furthermore, a transistor shows worse linearity in the subthreshold region (i.e., weak-inversion region) than in the strong-inversion region.

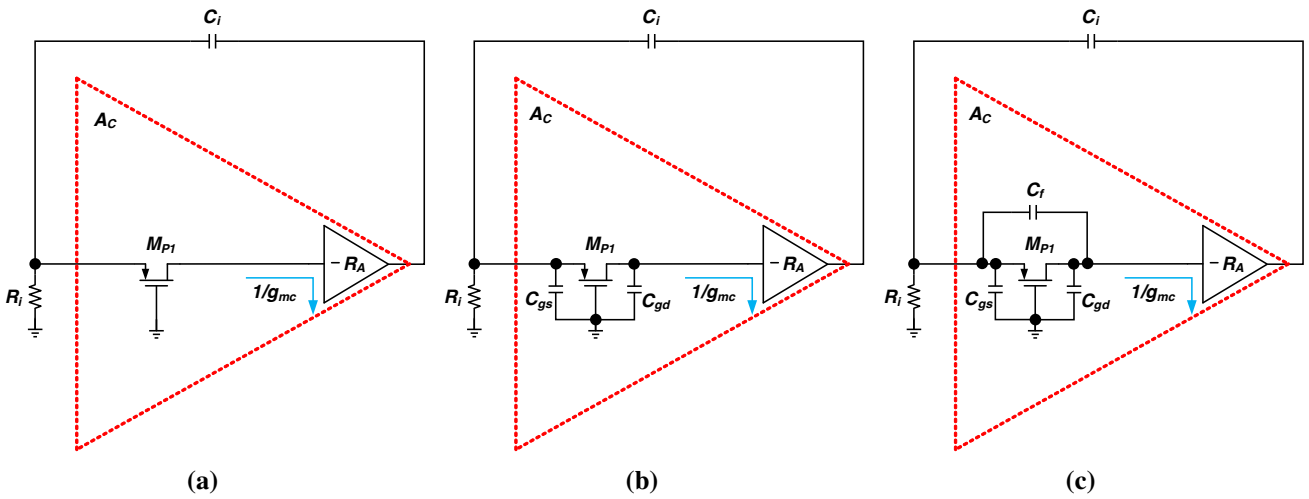

Fig. 9 The half circuit analysis for the CSB OTA-C integrator's loop gain without the parasitic gate capacitors (**a**), with the parasitic gate capacitors (**b**), and with both the parasitic gate capacitors and the feedforward compensation capacitor (**c**)

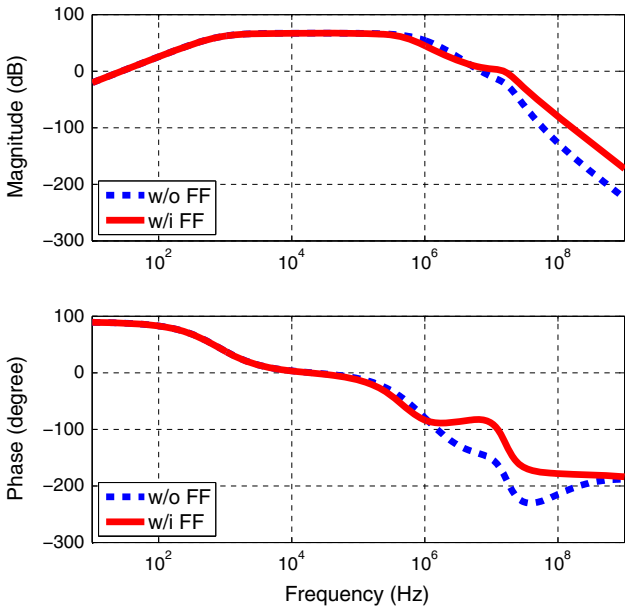

Fig. 10 The simulated magnitude (*top*) and phase (*bottom*) of the CSB OTA-C integrator's loop gain with (w/i) and without (w/o) the feedforward compensation capacitor C_f. As the loop gain has a zero at origin, the phase response starts from 90°

4.2 Voltage-sensing boosted OTA-C integrator

A voltage-sensing boosted (VSB) OTA-C integrator is proposed in [2], as shown in Fig. 6. As the OTA-C integrator shown in Fig. 1, it also has high input impedance and source-degenerated resistor R_i. However, this VSB OTA-C integrator has an inner negative feedback loop with an OPA to improve the linearity. The high-gain OPA acts to minimize its differential input voltage $(v_+ - v_-)$. Assuming $(v_+ - v_-) \approx 0$, the difference between the current from M_{P1} and M_{P2}, $(i_+ - i_-)$, is also approximately 0, because $(v_+ - v_-) = (i_+ - i_-)R_d$. Therefore, the source voltage of M_{P1}/M_{P2} precisely repeats the gate voltage, and the source degenerated structure is well linearized.

To investigate the details of the linearity, consider the VSB OTA-C integrator's transfer function:

$$H_V(s) = \frac{g_m R_d A}{1 + g_m R_d A} \cdot \frac{1 + sC_iR_i}{sC_iR_i + \dfrac{1 + g_mR_i}{1 + g_mR_dA}}, \tag{3}$$

where g_m is the transconductance of M_{P1}/M_{P2} and A is the voltage gain of the OPA. We find, in the VSB OTA-C integrator, if $g_mR_dA \gg 1$ and $R_dA/R_i \gg 1$, the transfer function becomes:

$$H_0(s) = 1 + \frac{1}{sR_iC_i}, \tag{4}$$

which has a term of 1 added to the ideal transfer function of an integrator. It means the output of the integrator is the sum of the integral of the input and the direct feedforward input. Because, for in-band audio signal, $1 \ll 1/sR_iC_i$, the local feedforward does not significantly affect the CT SDM's stability or dynamic range (DR) [17]. As the OPA is embedded in the OTA, compared with the active OTA-C integrator, the OPA's high gain A can be now utilized to achieve the high linearity for the *whole* integrator.

Therefore, if we increase g_mR_dA and R_dA/R_i, the VSB OTA-C integrator behaves like a linear integrator. As the time constant of the integrator is determined by the CT SDM's system-level design, reducing R_i will enlarge C_i. So, the value of R_i cannot be reduced aggressively. As a result, what we can do is to increase g_m, R_d and A for better linearity.

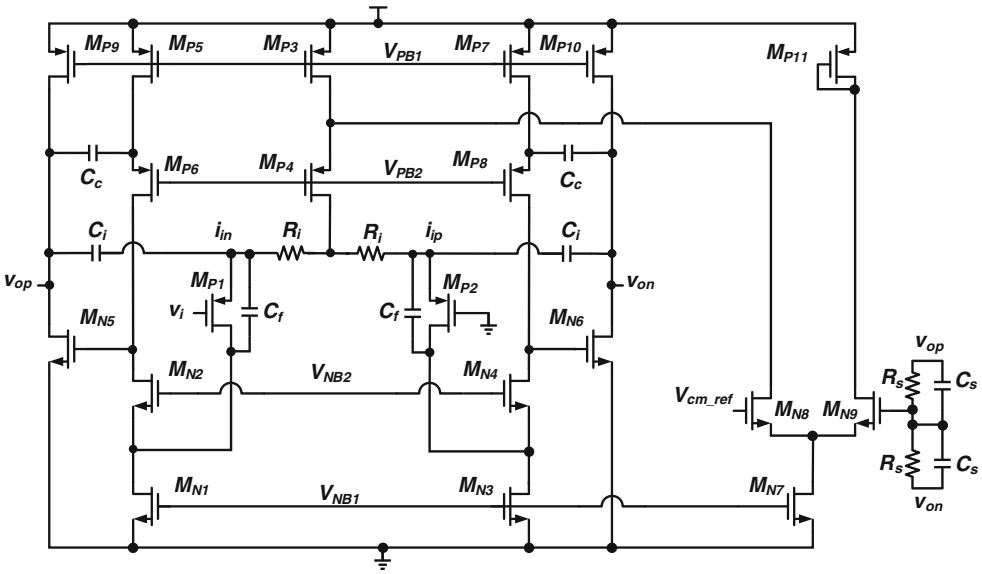

Fig. 11 The first integrator in the CT SDM based on the CSB OTA-C topology. Compared to the schematic shown in Fig. 8, the feedforward compensation capacitor C_f and the CMFB circuit are added for the complete circuit

Table 2 Critical circuit parameters in 1st integrator

R_i (kΩ)	20
C_i (pF)	15
C_c (pF)	0.3
C_f (pF)	12
$(W/L)_i$ (μm/μm)	3,600/0.5
$I_{b1,i}$ (μA)	3.5
$I_{b1,c}$ (μA)	1.0
I_{b2} (μA)	32.3

Increasing g_m can be achieved by increasing the bias current I_b (see footnote 1). As the DC voltage at the drain of M_{P1}/M_{P2} is given by $I_B R_d/2$, aggressively increasing I_b may make the drain voltage too high for the transistors to remain in saturation. So, we cannot increase g_m freely. Similarly, R_d cannot be greatly increased due to headroom limitations. Therefore, the values of g_m and R_d are limited by the headroom of the circuits, so that A needs to be large enough to compensate such limitation, in order to achieve the required linearity. The OPA is a two-stage amplifier [17], so that increasing A (at the frequency we are interested in) means increasing the speed of the OPA, so that it may increase power consumption or design complexity. Also, because g_m and the first stage's gain $g_m R_d$ both decrease, the noise from the integrator would increase.

In short, because of the voltage sensing, the VSB OTA-C integrator's g_m and R_d are limited by the need to maintain the proper ranges of the DC points, which may lead to more complex or more power consumptive OPA, as well as higher thermal noise. So, if we can avoid the voltage sensing by, for example, direct current sensing, we may have more design flexibility and possibly higher power efficiency to achieve the same linearity and noise.

4.3 Current-sensing boosted OTA-C integrator

The proposed CSB OTA-C integrator is shown in Fig. 7. While the OPA in the VSB OTA-C integrator was used to

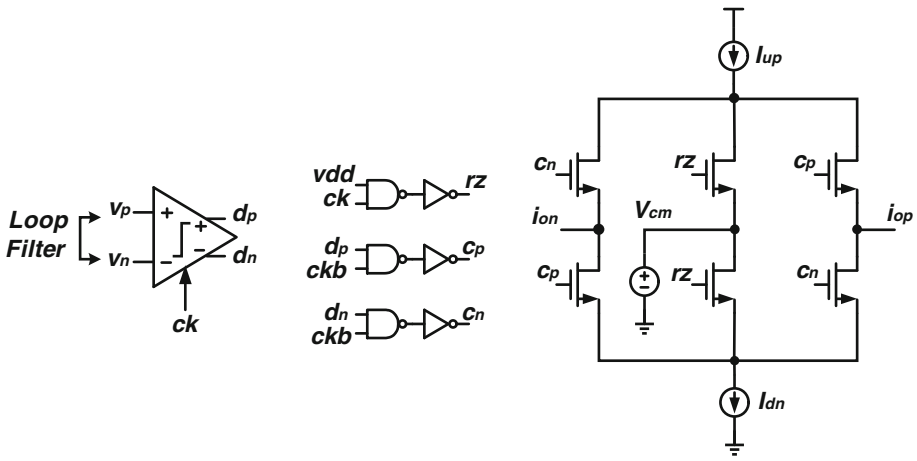

Fig. 12 The feedback RZ DAC in the CT SDM. The output digital code from the comparator is d_p and d_n (*left*), which will be passed through the logic gates along with the sampling clock signal *ck* and its complimentary signal *ckb* to get the control codes c_p, c_n and *rz* (*middle*). An 1-bit current-steering DAC is controlled by these codes to generate the feedback current signal (*right*)

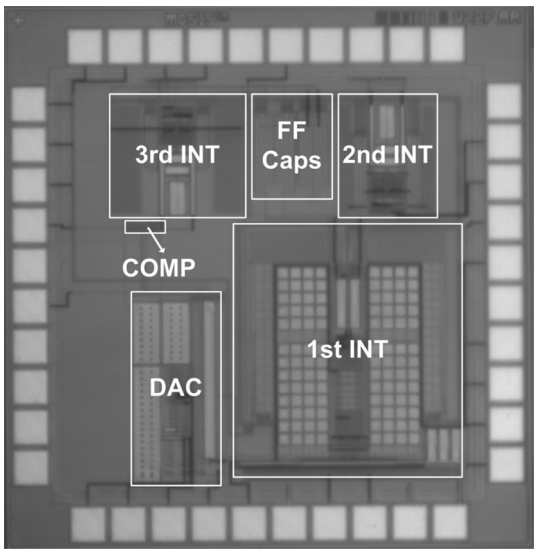

Fig. 13 The micrograph of the CT SDM in a 0.35-μm CMOS process. The total die size including the bonding pads is $1.35 \times 1.35\,\text{mm}^2$

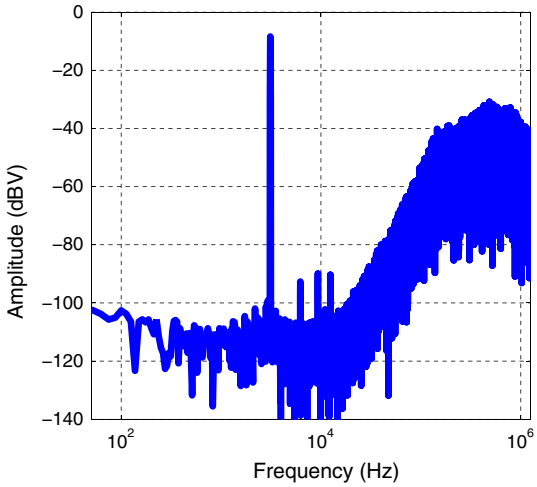

Fig. 14 The FFT plot of the measured output data with a Blackman window corresponding to the single-ended input amplitude of 128 mV_{rms} at 3.1 kHz, when the SNDR reaches its peak value. The bin size of the FFT is 12.5 Hz

force its input differential voltage to be small, in the CSB OTA-C integrator, we use a current-to-voltage converter with low input impedance to directly sense the difference current $(i_+ - i_-)$ from M_{P1} and M_{P2}. If the gain of the current-to-voltage converter, R_A (in ohms), is large enough, we can expect $(i_+ - i_-) \approx 0$, so that the source degenerated stage is well linearized as well.

The CSB OTA-C integrator's transfer function is shown as below:

$$H_C(s) = \frac{g_m R_A}{1 + g_m R_A} \cdot \frac{1 + sC_iR_i}{sC_iR_i + \dfrac{1 + g_mR_i}{1 + g_mR_A}}, \tag{5}$$

where g_m is the transconductance of M_{P1}/M_{P2}. We find, if we substitute R_dA with R_A, (3) becomes (5), so that the transfer function of the CSB OTA-C integrator is essentially the same as that of the VSB OTA-C integrator. Similarly, if $g_mR_A \gg 1$ and $R_A/R_i \gg 1$, the transfer function becomes (4) and the integrator is well linearized. For better linearity, we need to increase g_m and R_A. Because of the stability issues, the improvement of R_A is limited. However, we will see, in the proposed CSB OTA-C integrator, the value of g_m is flexible compared to the VSB OTA-C integrator.

A possible implementation of the current-to-voltage converter is the folded cascode stage shown in Fig. 8, where the source of M_{N2}/M_{N4} provides low input impedance for i_+/i_- to feed in. A second stage is needed to provide enough gain and output signal swing. The cascode compensation technique is used by connecting the output, v_{op}/v_{on}, to the source of M_{P6}/M_{P8} with a compensation capacitor C_c [18].

We can express the DC drain voltage of M_{P1}/M_{P2} as $V_D = V_{NB2} - V_{GS}$, where V_{NB2} is the gate voltage M_{N2}/M_{N4} that is determined by the bias circuitry, and V_{GS} is the gate-source voltage of M_{N2}/M_{N4} that can be determined by the bias current and size. When we change the bias current of M_{P1}/M_{P2}, I_B, we can change the bias current and/or the size of M_{N2}/M_{N4} to make V_D still be the desired value. So, increasing I_B can get higher g_m without affecting the DC points. Therefore, we have the flexibility to choose I_B to get high g_m for the needed linearity. As a result, the CSB OTA-C integrator has more design freedoms to choose the circuit parameters, which potentially leads to better performance including linearity.

The circuit design details and the complete schematic of the CSB OTA-C integrator will be discussed in Sect. 5.

5 Circuit implementation

5.1 First integrator

The first integrator is a CSB OTA-C integrator, whose basic concept has been shown in Fig. 8. However, as we will discuss below, the integrator has potential stability issues. We will analyze its stability and provide our solution to improve the stability. In addition, a common-mode feedback (CMFB) circuit is needed for this differential circuit.

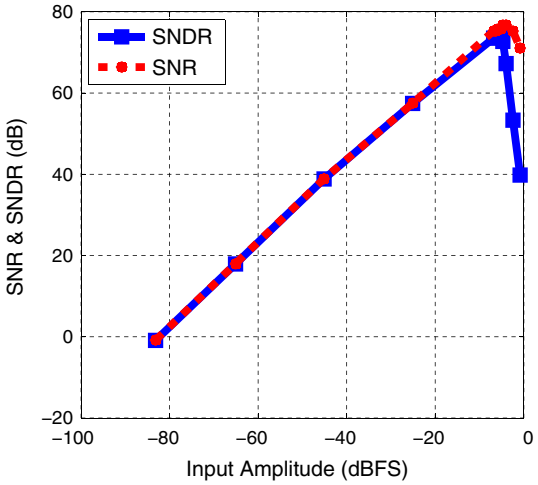

Fig. 15 The measured SNR and SNDR of the CT SDM versus the amplitude of a sinuoid input signal at 3.1 kHz. The full-scale amplitude is 360 mV in this design

We analyze the first integrator's stability with its half-circuit feedback loop, as shown in Fig. 9(a). If we treat M_{P1} and R_A as a whole amplifier ("feedforward amplifier") with a common-gate input stage, whose gain is $A_c = g_m R_A$ and input impedance is $R_{in} = 1/g_m$.

The loop gain of the feedback system is:

$$L_1 = \frac{sC_iR_A}{1 + \frac{1}{g_mR_i} + \frac{sC_i}{g_m}} \approx \frac{sC_iR_A}{1 + \frac{sC_i}{g_m}}, \tag{6}$$

where we assume $g_mR_i \gg 1$. If we set the DC value of R_A as R_0, R_A can be expressed as:

$$R_A = \frac{R_0}{(1 + s/p_1)(1 + s/p_3)}. \tag{7}$$

The expressions of the poles are [18]:

$$p_1 = \frac{1}{g_{m2}r_{o2}r_{o1}C_c}, \tag{8}$$

$$p_3 = \frac{C_c}{C_{o1}} \cdot \frac{g_{m2}}{C_i}, \tag{9}$$

where g_{m2} is the transconductance of M_{N5}/M_{N6}, r_{o1} is the output resistance at the drain of M_{N2}/M_{N4}, r_{o2} is the output impedance of the output stage of the current-to-voltage converter, and C_{o1} is the capacitance at the gate of M_{N5}/M_{N6}.

Therefore, L_1 can be further expressed as:

$$L_1 = \frac{s/\omega_0}{(1 + s/p_1)(1 + s/p_2)(1 + s/p_3)}, \tag{10}$$

where ω_0 and p_2 are expressed as:

$$\omega_0 = \frac{1}{R_0C_i}, \tag{11}$$

$$p_2 = \frac{g_m}{C_i}. \tag{12}$$

The loop gain has three poles and one zero (at zero frequency). Because the lower-frequency pole p_1 will be compensated by the zero, the magnitude of the loop gain becomes flat after p_1. The two poles p_2 and p_3 at higher frequency will make the loop gain roll off. If p_2 and p_3 are well separated, the system will be stable.

In this design, the size of M_{P1} and M_{P2} is made large enough to get lower flicker noise, better matching and higher g_m for given bias current, so that their parasitic capacitors C_{gs} and C_{gd} become large enough to affect the circuit. With C_{gs} and C_{gd}, the loop gain of the half circuit in Fig. 9(b) is:

$$L_2 = \frac{s/\omega_0}{(1 + s/p_1)(1 + s/p_2')(1 + s/p_3)(1 + s/p_4)}, \tag{13}$$

where

$$p_2' = \frac{g_m}{C_i + C_{gs}}, \tag{14}$$

$$p_4 = \frac{g_{mc}}{C_{gd}}, \tag{15}$$

g_{mc} is the input conductance of the current-to-voltage converter, which is the transconductance of M_{N2}/M_{N4}. We find an additional pole p_4 is introduced by C_{gd}. In the loop, $z_0 = 0$ and p_1 cancels each other at low frequency. The loop stability will mostly be determined by p_2', p_3 and p_4. Because C_i is selected to be large for a smaller R_i and smaller noise, it is difficult to make p_3 very high. Also, because C_{gd} becomes more significant with large transistor size, p_4 may be close to p_3. Considering p_2' has already introduced 90-degree phase shift, the phase margin of the loop gain may be limited due to closely spaced p_3 and p_4, because the phase response is sensitive to poles.

The magnitude and phase response of the loop gain in this design is shown in Fig. 10, where the phase margin is only 36°. Therefore, the additional pole p_4 degrades the stability. We could aggressively increase either p_3 or p_4 to get better stability, but considerably more power consumption would be needed.

Instead of directly increasing the poles' frequency, we compensate the effect of the additional pole p_4 by adding a feedforward capacitor C_f in parallel with the input transistor's source and drain, as shown in Fig. 9(c), and the loop gain becomes:

$$L_3 = \frac{s/\omega_0(1+s/z_1)}{(1+s/p_1)(1+s/p_2^{''})(1+s/p_3)(1+s/p_4^{'})}, \quad (16)$$

where

$$z_1 = \frac{g_m}{C_f}, \quad (17)$$

$$p_2^{''} = \frac{g_m}{C_i + C_f + C_{gs}}, \quad (18)$$

$$p_4^{'} = \frac{g_{mc}}{(C_{gs}+C_i)||C_f}, \quad (19)$$

assuming that $C_{gd} \ll C_{gs}, C_i, C_f$. We find that $p_2^{'}$ shrinks to $p_2^{''}$ due to C_f. Also, p_4 becomes $p_4^{'}$, which is not related (actually weakly related) to C_{gd}, because the feedforward path connects C_f, C_{gs} and C_i, making a large equivalent capacitor $(C_{gs}+C_i)||C_f$ that can absorb C_{gd}. Because $p_4^{'}$ is smaller than p_4, it could make the stability discussed above even worse. However, the most important effect of C_f is that an additional zero z_1 is now available to compensate the additional pole $p_4^{'}$ brought by the parasitic capacitance of the input transistors. Therefore, the phase margin will be improved.

According to Fig. 10, in this design, the phase margin of the loop gain with C_f becomes 61°, so that the capacitive feedforward compensation improves the stability.

The first integrator with the feedforward capacitor and a common-mode feedback (CMFB) circuit is shown in Fig. 11. Its CMFB circuit measures the difference between the output CM voltage and the reference voltage, and converts the voltage difference to a current, which controls the bias current of the integrator's first stage [19].

The critical circuit parameters are shown in Table 2, where $(W/L)_i$ is the size of the input differential pair (M_{P1}/M_{P2}), $I_{b1,i}$ is the bias current of the input differential pair, $I_{b1,c}$ is the folded cascode stage's bias current and I_{b2} is the output stage's bias current.

5.2 Second and third integrators

The second and third active-RC integrators are both based on a typical two-stage OPA with a cascode amplifier as the first stage and a common-source amplifier as the second stage [20]. The third integrator is also used to implement the feedforward summation (see Fig. 4).

5.3 Comparator

The comparator in the SDM is a typical dynamic comparator that consists of a latched amplifier and an RS latch [21]. The comparator has relaxed requirement on the offset, so that no preamplifier is needed.

5.4 Feedback DAC

The feedback DAC is an 1-bit current-steering RZ DAC with 50 % pulse width [2], as shown in Fig. 12. The output codes of the comparator, with the clock signals, pass the logic gates to generate the control codes for the switched current source and implement the RZ feedback waveform. At the RZ phase, the control signal rz is high, so that no current will be fed back to the loop filter. A common-mode DC voltage (the nominal value is the middle voltage between the power supply and ground) is connected to the middle of two RZ switches [22].

6 Measurement results

The CT SDM was fabricated with a 0.35-μm CMOS process, and its micrograph is shown in Fig. 13. The system can be powered with a voltage supply of 2.8–3 V.

The fast Fourier transform (FFT) plot of the measured output data is shown in Fig. 14, corresponding to a single-ended input sinusoid with amplitude of $V_P = 182$ mV and frequency of 3.1 kHz. The signal-to-noise ratio (SNR) is 75.7 dB and the SNDR is 74.2 dB (the peak value that the CT SDM can achieve). Noise and distortion were calculated from 200 to 10 kHz. Unlike the CT SDMs with fully differential input signals that can achieve very low second-order harmonics, our CT SDM shows considerable second-order harmonic due to its single-ended input. The third-order harmonic primarily comes from the nonlinearities of the transistors, similar to other CT SDMs even with fully differential input.

The measured relationship between the input amplitude and SNR/SNDR is shown in Fig. 15. The peak SNR is 75.8 dB, peak SNDR is 74.2 dB and DR is 83.2 dB.

The total power consumption of the CT SDM based microphone readout interface is 801 μW, and it should be noted that it directly drives the logic analyzer's probe with an 8.5-pF input capacitance [23] by an on-chip buffer (i.e., inverter chain), whose power consumption is around 171 μW. Therefore, the CT SDM core consumes about 630 μW.

The performance of this CT SDM based microphone readout interface is summarized and compared with other microphone readout circuits with *single-ended input and high input impedance* in Table 3, where the FoM is defined as:

$$\text{FoM} = \frac{\text{P}}{2\text{BW} \cdot 2^{\text{ENOB}}}. \quad (20)$$

Table 3 Performance summary and comparison

	This work	[6]	[7, 24]	[1]	[2]
CMOS process (μm)	0.35	0.35	0.35	0.13	0.5
Peak SNDR (dB)	74	78	53†	60	62
DR (dB)	83	98	80†	75	80
Input Amplitude with Peak SNDR (mV_{rms})	127	150	1.6	16	88
BW (kHz)	10	20	20	25	11
Power consumption (μW)	630	6,100	378	600	1,080
Voltage supply (V)	2.8	3.0	1.8	3.3	1.8
ENOB	12.0	12.7	8.5	9.7	10.0
FoM (pJ/level)	7.7	22.9	26.1†	14.4	47.9

$$\text{FoM} = \frac{\text{Power consumption}}{2\text{BW} \cdot 2^{\text{ENOB}}}$$

† The noise in this design is A-weighted. The unweighted noise is normally higher, and the corresponding unweighted peak SNDR and FoM would be considerably degraded

BW is the SDM's bandwidth and P is the power consumption.

7 Conclusions

The microphone readout interface circuit proposed in this paper employs a CT SDM to directly read the signal from a MEMS microphone. The first integrator is a boosted OTA-C integrator with current sensing and feedforward compensation techniques, to address the special requirements on the high input impedance and high linearity with a single-ended input. The current sensing by the folded-cascode stage decouples the tradeoff between DC points and circuit performance, and the feedforward capacitive compensation effectively increases the integrator's stability without directly increasing the power consumption.

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