Current Conveyor Based Wide-band Current Driver for Electrical Impedance Tomography

Arun Rao, *Student Member, IEEE*, and Kofi Odame, *Senior Member, IEEE*

***Abstract*—Electrical Impedance Tomography (EIT) for prostate and breast cancer detection require wide-band ac current drivers which can deliver current up to 10MHz. The current drivers should exhibit low harmonic distortion and provide accurate current to the tissue being examined. This work presents an integrated current driver which can deliver 1.2mA of current up to frequencies of 10MHz. The current source was fabricated in CMOS 0.18-μm technology with a power supply of 3.3V, and occupies a core area of 0.26mm^2. The measured harmonic distortion for a peak current of 1.2mA is < 0.1$\%$ for frequencies less than 100kHz, and increases to 0.68$\%$ at 10MHz. The output impedance measured is 101$k\Omega$ at 1MHz and 19.5$k\Omega$ at 10MHz. The circuit is suitable for high frequency small form factor EIT systems.**

***Index Terms*—bioimpedance, current conveyor, gain boosted cascode, integrated current driver, electrical impedance tomography, wide-band, CMOS circuits.**

I. Introduction

Electrical impedance varies widely between cancerous and benign tissues and exhibits frequency dependent characteristics which have been used for differentiating various kinds of cancer [1]. Electrical Impedance Tomography (EIT) is an imaging modality that incorporates the bioimpedances of various parts of the measured tissue to provide a spatial mapping of the organ being probed. By injecting a sinusoidal current into the tissue at the source electrode and measuring the voltages induced at the remaning electrodes, impedance of tissue is obtained. One of the key advantages of an EIT system is its relatively smaller size and inexpensive cost compared to other imaging techniques such as Magnetic Resonance Imaging (MRI) or Computerized Tomography (CT). EIT is also non-invasive and non radiative, which are desireable.

A major challenge of EIT is that it requires an accurate, high output impedance current driver to deliver a pure sinusoidal signal to the tissue under test. The EIT current driver has traditionally been implemented as a Howland current source with discrete components [2]. This implementation unfortunately introduces a significant amount of parasitic capacitance, which limits the bandwidth of the EIT system. To achieve higher frequencies of operation, the current driver must be implemented in an integrated circuit (IC), as part of an active electrode system, whereby the electronics are physically close to the electrodes and parasitic capacitance is minimized. Several promising IC current drivers have recently been proposed [3], [4], [5], [6]. Unfortunately, none of the solutions reported in the literature can operate beyond the 1 MHz range, where electrical impedance interrogation of intracellular physiology could provide increased contrast between benign and cancerous tissue [7], [8].

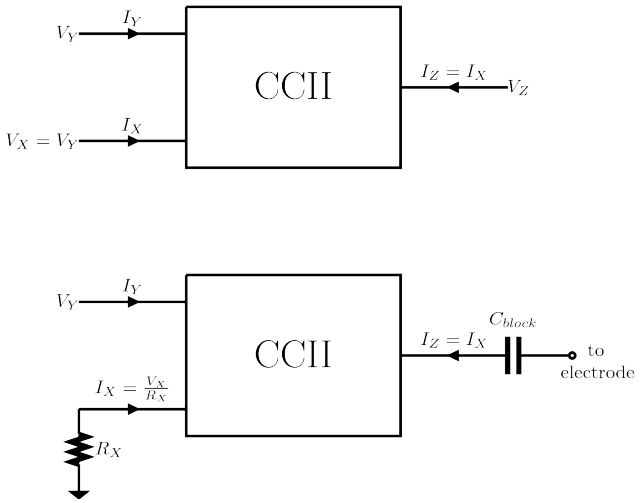

Figure 1. Block diagram of current conveyor is shown in the top figure. (a) The voltage induced at terminal X follows terminal Y. The current delivered at terminal Z is such that $I_Z = I_X$. (b) The figure at the bottom shows the implementation of the current driver. A resistor at terminal X generates the current delivered at terminal Z to the tissue using a DC blocking capacitor C_{block}.

In this paper an integrated CMOS current conveyor based wide-band current source is introduced. Compensation for high speed operation at the transconductance stage is achieved using indirect compensation technique [9] which enables operation up to 10MHz. Current mode circuits [10] at the output stage further aid in the wide-band operation of the designed current source.

This paper is structured as follows. An overview of the architecture and solution is described in Section II. Section III provides detailed design and analysis of the circuits employed. Section IV provides details of the experimental setup and measured results. Section V discusses details on the measured results, contributions and Section VI provides the conclusions.

II. Overview

Figure 1 shows the block diagram of the CCII current conveyor [11], which can be classified as a 3 port network with terminals X, Y and Z. Voltage induced at terminal X follows the voltage applied at terminal Y which has infinite input impedance. Positive and negative currents are delivered to the high output impedance node of terminal Z through terminal X.

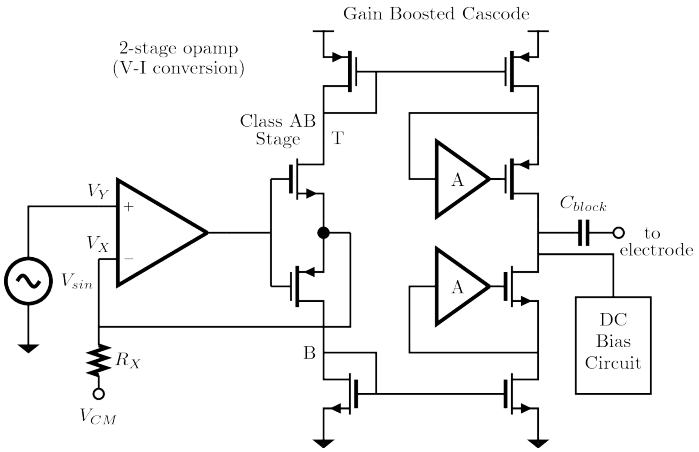

Figure 2. The architecture of the current driver. (a) The voltage to current conversion is performed using a 2-stage opamp with indirect feedback compensation. (b) Class AB output stage at the output of the opamp is necessary for generating the sinusoidal current at terminal X using a resistor R_X. (c) Current is mirrored to the high output impedance terminal Z with a gain enhanced current mirror forming the output stage.

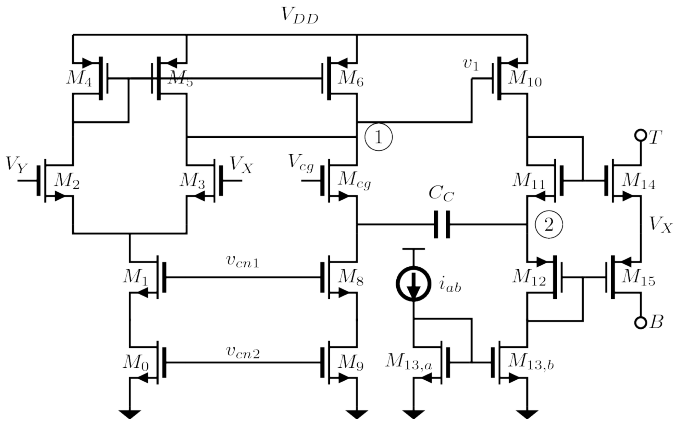

Figure 3. 2-stage opamp with indirect compensation followed by a class AB output stage. (a) The current from the output node 2 is indirectly fed to node 1 using the commoon gate transistor M_{cg}. This forms the indirect feedback compensation technique. (b) Transistors $M_{11}, M_{12}, M_{14}, M_{15}$ form the class AB output stage to source and sink currents into node X.

Figure 2 shows the architecture of the implemented current source which is based on [12]. The voltage to current conversion is performed using a 2-stage opamp in unity gain configuration. The use of indirect compensation technique helps achieve high bandwidth up to 10MHz. A class AB buffer at the output of the 2-stage opamp creates a low impedance node at the output, necessary for the generation of current at terminal X using the resistor R_X. The current generated at terminal X is mirrored to the high output impedance node terminal Z through a gain enhanced cascode current mirror to provide high linearity and high output impedance for high frequency operation [13], [14], [15]. The current driver is designed to inject a current of $1.2mA$ while maintaining less than 1% harmonic distortion over the desired frequency range.

III. Circuit Design and Analysis

A. V-I conversion

Figure 3 shows the circuit diagram of the 2-stage op-amp with indirect compensation technique used for the voltage to current conversion in the current driver. A RHP pole zero appears in the transfer function of a conventional 2-stage opamp compensated using a compensation capacitor C_c. This problem has been well studied and various compensation techniques exist to cancel the RHP zero or move it into the LHP to improve stability. However, nulling resistor technique for compensation is process dependent and the use of transistor in triode region of operation can cause issues with large signal behavior [16]. Also, the value of compensation capacitor required for compensation is high which limits the speed of the circuit. In the indirect compensation technique the compensation capacitor is not directly connected to the opamp output. Instead, pole-splitting is achieved indirectly using a common gate transistor, M_{cg}, feeding the current from the output back to the first stage. Input transistors M_2, M_3, with current mirror loads M_4, M_5 and cascoded tail transistors M_0, M_1 form the input stage of the 2 stage opamp. The gain of the input stage is given by $A_{v1} = g_{m2}(r_{o3}||r_{o5})$, where $g_{m2} = g_{m3} = G_{M1}$ are the transconductances of the input differential pair and r_{o3}, r_{o5} are the ouput impedances of transistors M_3, M_5 respectively. The branch comprising of transistors M_6, M_8, M_9, and M_{cg} form the indirect compensation branch in the circuit along with the compensation capacitor C_c. The gate of the common gate transistor M_{cg} is tied to the common mode voltage of the circuit. The currents in the input differential pair transistors and the indirect feedback branch are kept equal to achieve $G_{m1} = g_{m,cg}$. The output branch which provides the second stage gain is provided by transistors M_{10} and M_{13} which is the current source load. The gain is given by, $A_{v2} = g_{m10}(r_{o10}||r_{o13})$, where g_{m10} is the transconductance of transistor M_{10} and r_{o10}, r_{o13} are the output impedances of transistors M_{10}, M_{13} respectively. The bias voltages v_{cn1} and v_{cn2} are provided using a wide swing cascode current mirror [17] (not shown). Class AB output buffer stage is formed by transistors M_{11}, M_{12}, M_{14}, and M_{15}. When voltage, v_1, at the gate of transistor M_{10} increases, M_{15} turns on and M_{14} turns off, as the gates of M_{11} and M_{12} move towards GND. Similarly, M_{14} sources all the current when v_1 decreases, which implies a class AB operation. The current source i_{ab} provides the necessary DC current bias for the class AB output branch.

B. Gain Boosted Cascode Output Stage

The high output impedance necessary for the current driver is achieved by using the structure shown in Fig. 4. Since the amplifier used here is auxillary in nature, its frequency behavior should not affect the overall high bandwidth requirements of the current driver. The amplifier should have high unity gain frequency and exhibit single pole behavior and the closed loop response at the output branch should be stable. To achieve these specifications a common source amplifier, with a current source load is used to implement the gain stage. With the included gain

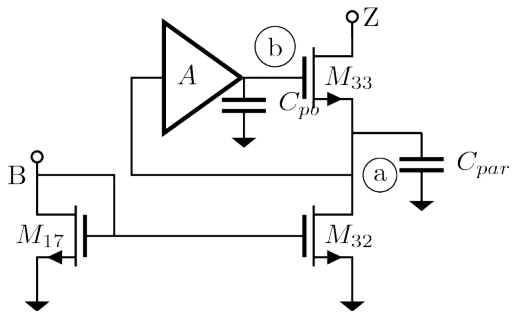

Figure 4. The gain boosted cascode structure with the amplifier 'A' providing an overall output impedance of $Ag_{m2}r_{o2}r_{o1}$ at node Z.

boosting amplifier , the overall circuit of the output stage is shown in fig. 5. The positive and negative currents generated at node X, in the V-I conversion stage is mirrored by the transistors M_{16}, and M_{17}. The output branch delivering current is formed by transistors M_{24} and M_{25} in the PMOS branch and transistors M_{32} and M_{33} in the NMOS branch. Gain boosting for the PMOS branch is achieved using transistors M_{18} - M_{23} and M_{26} - M_{31} for the NMOS branch. The common source amplifier with its current source load for both branches can be identified as transistors M_{21}/M_{29} and M_{23}/M_{31} respectively. For a more detailed analysis, the reader is referred to [15]. The gain from the PMOS and NMOS gain boosting amplifiers is given by the following equations :

$$A_{gb,P} = g_{m21}(r_{o21}//r_{o23}) \tag{1}$$

$$A_{gb,N} = g_{m29}(r_{o29}//r_{o31}) \tag{2}$$

where $A_{gb,P}$ and $A_{gb,N}$ are the gains from gain boosting amplifiers of the PMOS and NMOS branch respectively. From equations 1, and 2, the overall output impedance at node Z, can be written as,

$$Z_{out} = (g_{m25}r_{o25}r_{o24}g_{m21}(r_{o21}//r_{o23}))// \\ (g_{m33}r_{o33}r_{o32}g_{m29}(r_{o29}//r_{o31}))$$

C. DC Bias Circuit

The current drivers used in EIT applications have a DC blocking capacitor, to ensure no DC current flows into the human tissue. This results in an equivalent structure at the output stage as shown in fig. 6. The current sources in the NMOS and PMOS branches of the output stage will result in an undefined voltage at node Z, and result in unreliable operation. For proper operation of the current driver such that all transistors are in saturation we devise a feedback structure which will keep the current driver in the proper operating regime. This structure is shown in Fig. 7. Here the output branch of the current driver is shown where an OTA sets the output common mode voltage to V_{CM}. The OTA is implemented as a current mirror OTA with

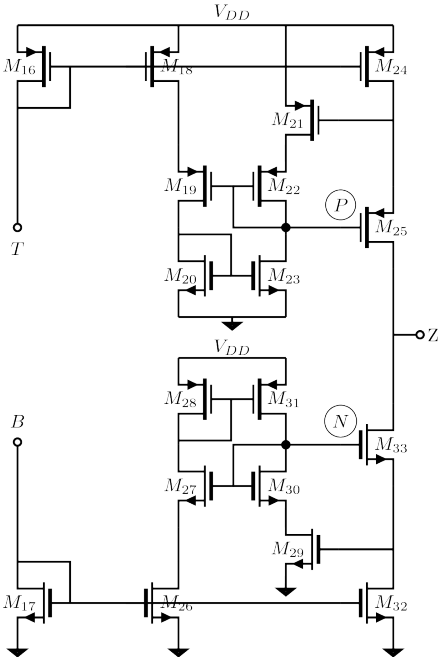

Figure 5. Mirroring of current generated at node X to output node Z using a gain boosted cascode structure. Tha auxillary amplifiers for the gain boosted casocode structure have a single pole nature to enable high frequency operation.

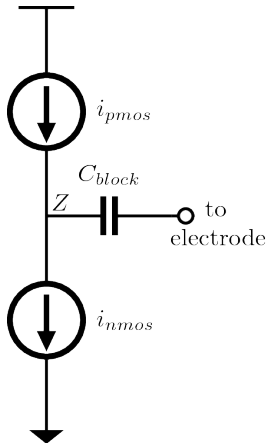

Figure 6. With a DC blocking capacitor C_{block}, the output branch of the current drivers consists of PMOS and NMOS current sources in series, which will cause unreliable operation.

input transistors sized to minimize the capacitive loading at node Z. The transistor, M_{FB}, is sized such that its drive effects at node a are negligible during normal operation, as its inclusion here is for the sole purpose of setting the output common mode level. For our design we have sized M_{FB} to be $1/30$, the width of transistor M_{32}. The length of the transistor remains the same as transistor M_{32}, to ensure that the output resistance achieved is the same.

D. Frequency Response and Analysis

The frequency response of the 2-stage amplifier shown in Fig. 3, can be studied from the small signal equivalent circuit given

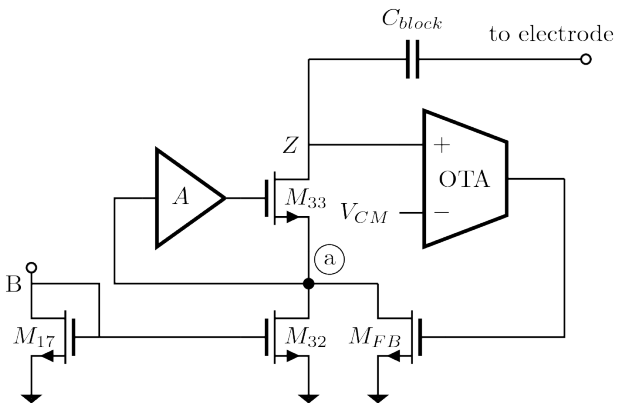

Figure 7. The figure shows the structure designed to keep the current driver in the proper operating regime. The OTA at the output stage sets the output voltage to the common mode reference voltage V_{CM}, which ensures that all the transistors in the output branch of the current source structure are in saturation thus enabling reliable operation.

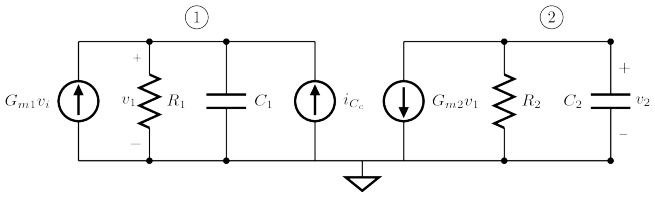

Figure 8. Small signal model for analysis of indirect compensation is shown. Nodes 1 and 2 represent the output of the first and second stage of the 2-stage opamp used for V-I conversion. R_1, R_2, and C_1, C_2 are the equivalent output resistances and capacitances seen at the output of stage 1 and 2 respectively. The current indirectly fed from the output stage to node 1 is shown as i_{C_c} and given by Eq. 3.

in Fig. 8. The current through the compensation capacitor can be obtained as follows,

$$i_{C_C} = \frac{v_2 - v_1}{1/j\omega C_c + 1/g_{m,cg}} \tag{3}$$

where, v_1, v_2 are the output voltages of stage 1, 2 respectively, $g_{m,cg}$ is the transconductance of the common gate transistor M_{cg}. Now, $v_1 = \frac{v_2}{A_{v2}}$, and assuming A_{v2} is large, Eq. (3) can be approximated as, $i_{C_c} = \frac{v_2}{1/j\omega C_c + 1/g_{m,cg}}$. The transfer function from output of the second stage to the input is given by the following equation,

$$\frac{v_2}{v_i} = \frac{-G_{m1}R_1G_{m2}R_2(1 + s\frac{C_c}{g_{m,cg}})}{s^2(R_1C_1R_2C_2) + s(R_1C_1 + R_2C_2 + R_1G_{m2}R_2C_c) + 1} \tag{4}$$

Here G_{mi}, R_i, C_i are the equivalent transconductances, output resistance and capacitances, where $i = 1, 2$ for stages $1, 2$ of the 2-stage opamp. From Eq. (4), we identify a LHP zero located at,

$$f_z = \frac{g_{m,cg}}{2\pi C_c} \tag{5}$$

Note that the zero occurs approximately at the unity gain frequency of the opamp given by $f_{ug} = \frac{G_{m1}}{2\pi Cc}$, assuming equal transconductances from transitors $M_{2,3}$ and M_{cg}. The phase margin at unity gain frequency is being enhanced by the left half plane zero which adds to the overall phase response. The coefficient of s term in the denominator of Eq. (4) can be approximated to $R_1G_{m2}R_2C_c$. The capacitance seen at node 2, are the parastic capacitances of transistors M_{11}, M_{12} and hence the term R_2C_2 is small. Thus the second pole occurs at,

$$f_2 = \frac{G_{m2}C_c}{2\pi C_1C_2} \tag{6}$$

Equation (6) shows that the location of second pole is at a much higher frequency compared to conventional miller compensation techniques. The indirect feedback of current though the compensation capacitor C_c and the common gate amplifier M_{cg} enables the 2-stage opamp to operate at higher frequencies necessary for the current driver.

The frequency response of the gain boosting amplifier is also of importance in the output stage. It is necessary to ensure that the gain boosting amplifier has a unity gain bandwidth much greater than the desired frequency of operation of the current driver. This also ensures that the feedback loop of the auxillary amplifiers formed at the output stage is stable and does not oscillate. The gain boosting common source amplifer is formed by transistors M_{21-23} and M_{29-31} for the PMOS and NMOS branches respectively. The unity gain frequency is given by $f_{u,gb} = \frac{g_{m,cs}}{2\pi C_{par}}$, where $f_{u,gb}$ represents the unity gain frequency of the PMOS or NMOS gain boosting amplifiers, $g_{m,cs}$ are the transconductances of common source ampifiers M_{21}, M_{29}, and C_{par} are the capacitances at node P, N as shown in Fig. 5. Stable operation of the gain boosting loop is achieved by maximizing the transconductance and sizing transistors such that the parasitic capacitances at node P, N is reduced. Sizing of transistors M_{25}, M_{33} is critical as its parasitic capacitance affects the output terminal Z as well. Lower parasitics at the output terminal is necessary for the current driver's high frequency operation. By using minimum channel devices for transistors M_{25}, and M_{33} we ensure that the parastics at node P, N and output terminal Z are reduced.

IV. Measured Results

The current driver was fabricated in XFAB 0.18-μm XH018 CMOS process with supply voltage of 3.3V [18]. Design, layout and simulation was performed using Virtuoso Cadence. On-chip resistor of 500Ω was fabricated to generate the current at the V-I conversion phase as shown in Fig. 2. Two additional current source test structures were also designed and included in the chip for complete measurement. The current driver core area with test structures is approximately $0.26mm^2$ as shown in Fig. 9. The chip was tested on a custom built PCB with required external current sources for biasing.

Figure 10 shows the output current vs frequency plot for the current driver at various current levels with a load of 500Ω. The input signals to the current driver was generated using a Kiethley Instruments 3300 waveform generator capable of generating sinusoidal signals greater than 10MHz with negligible distortion

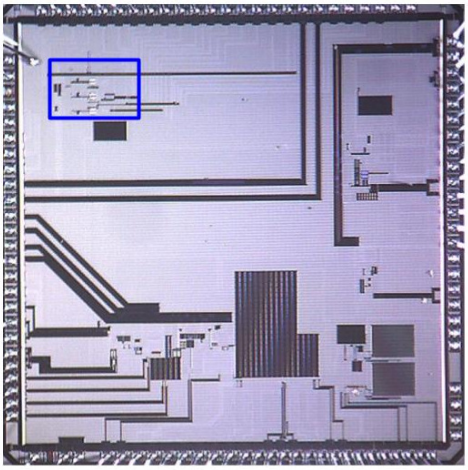

Figure 9. Chip Microphotograph. The current driver with test structures is indicated by the blue rectangle.

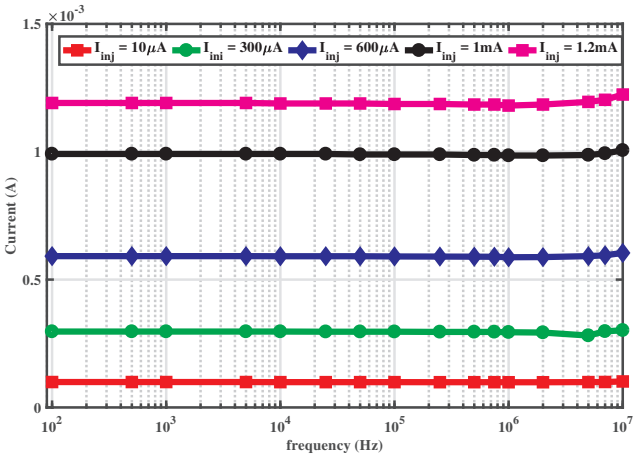

Figure 10. Output current vs frequency for the current driver with curent levels of $100\mu A$, $300\mu A$, $600\mu A$, $1mA$ and $1.2mA$. A 500Ω resistor was used as the load.

contributed to measurements. A $600mV$ peak to peak voltage at the input terminal Y generates the maximum current of $1.2mA$ at terminal Z. The output voltage at the load was monitored using a Rigol 1104-Z oscilloscope. The accuracy of the current source measured are 0.21%, 0.46%, and 2.68% for frequency ranges of 100Hz - 100kHz, 100kHz - 1MHz, and 1MHz - 10MHz respectively for current level of $600\mu A$. Whereas, with an output current of $1mA$ the accuracies are 0.2%, 0.4%, and 2.03% for frequency ranges of 100Hz - 100kHz, 100kHz - 1MHz, and 1MHz - 10MHz respectively. Figure 11 shows the measured THD values against frequencies. Current values of $1mA$, and $1.2mA$ are chosen to show the performance of the current driver with a 500Ω load. The current driver achieves a THD of less than approximately 0.7% harmonic distortion at 10MHz while delivering a current of $1.2mA$ to the load.

A Stanford Research Systems SRS 785 spectrum analyzer was used for noise measurements of the current driver. Due to limitations of the equipment, noise was measured upto

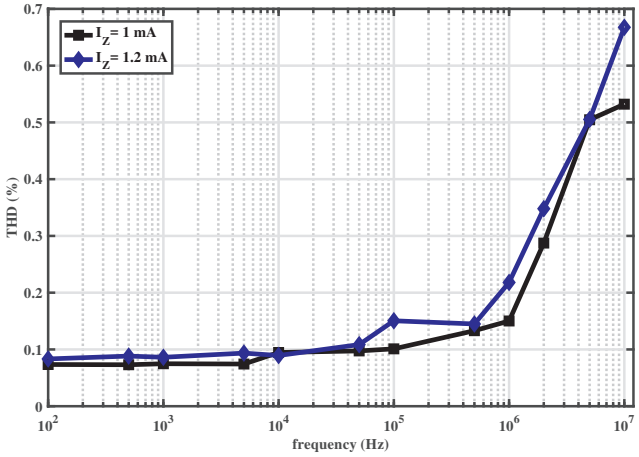

Figure 11. Plot showing the THD vs frequency for current levels $1mA$ and $1.2mA$. The worst harmonic distortion measured for the current driver is approximately 0.7%.

100kHz. Figure 12 shows the comparison of measured noise with respect to cadence simulations. The total integrated noise at the output was approximately $658\mu V$ determined by simulation. The output compliance voltage of the current source was also measured by using a $1k\Omega$ load and varying the input voltage amplitudes. The current driver has a output voltage compliance of 0.7V.

The measurement of the output impedance of the current driver was performed as described in [19]. The test configuration uses a Linear Technology LT1806 wide bandwidth precision opamp as a negative feedback amplifier. Resistors with 0.1% precision were used on the PCB for the calibration and feedback resistors. The associated parasitics of the board was measured using a Instek 821 precision LCR meter. The measured board parasitics, along with the output pad capacitance of the chip (terminal Z), was incorporated into the calculation of the output impedance. An average of 2500 points for a single frequency point measurement was used to obtain reliable measurement data. Figure 13 shows the output impedance vs frequency for the current driver. The output impedance is $101k\Omega$ at 1 MHz, and $19.5k\Omega$ at 10 MHz. At a frequency of 10MHz the output impedance of current source is much higher than tissue impedance, such that current from the driver can be injected into the current source with minimal loss in accuracy.

V. Discussion

Since the number of pads available on the chip was limited, the output pad for current injection from the current driver at terminal Z could not be sufficiently isolated on chip. This caused additional coupling capacitance with adjacent signals on chip, which would degrade high frequency output impedance of the current driver. The output impedance measurement for the test chip setup is also sensitive to board parasitics and prone to errors. To minimize the error in measurements, each measured data point on the output impedance vs frequency graph has 2500 values averaged. The method of measurement reported in [19]

Table I
MEASURED PERFORMANCE AND COMPARISON.

Parameter	[3]	[5]	[6]	This Work
Bandwidth	90kHz	$\leq$1MHz	$\leq$200kHz	**100Hz - 10MHz**
Output Impedance	> 560 $k\Omega$ @ 90kHz	**360$k\Omega$** @ 1MHz	–	101$k\Omega$ @ 1MHz, 19.5$k\Omega$ @ 10 MHz
Max. Output Current (peak-peak)	350μA	1mA	1mA	**1.2mA**
THD (frequency)	0.81% @ 250μA (Unknown)	< 0.1% @ 1mA (50kHz)	< 0.1% @ 0.1mA (Unknown)	**< 0.1%** @ 1.2mA (50kHz) < 0.7% @ 1.2mA (10MHz)
Voltage Compliance (Power Supply)	1.5 V (1.5 V)	**$\pm$2 V** ($\pm$2.5 V)	– (1.8 V)	0.7 V (3.3 V)

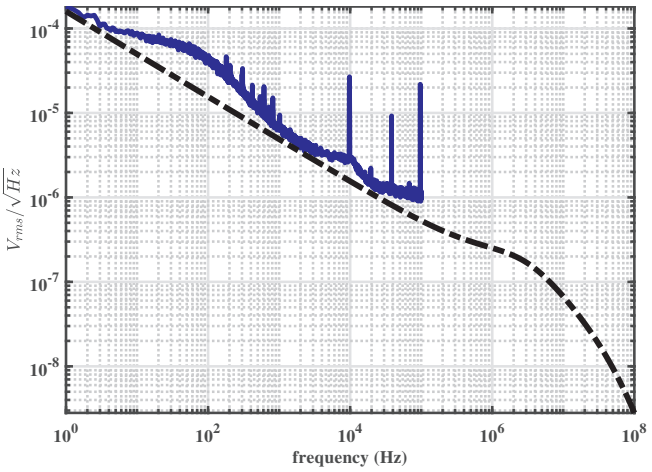

Figure 12. Plot showing the simulated vs measured result of the noise at the output of the current driver. Blue dashed line represents the simulated result using cadence.

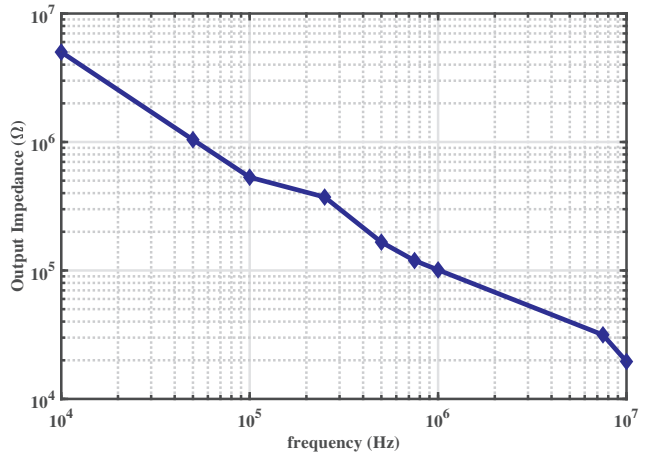

Figure 13. Output impedance vs frequency for the current driver. The measured output impedance is 101$k\Omega$ at 1MHz, and 19.5$k\Omega$ at 10MHz.

has a generalized impedance converter and tuning methods not available in our present setup. Also the values of resistors chosen could not measure impedance values lower than 10kHz.

The current driver achieves wide-band operation up to 10MHz, necessary for EIT prostate and breast cancer detection. The THD values achieved are an improvement from previously reported integrated designs. The use of indirect feedback compensation enables the use of smaller compensation capacitor and thus reducing the area for wide-band operation. This would help inclusion of the current driver in active electrode systems. The current delivered to the load is 1.2mA at 10MHz. The comparison with preciously reported current drivers is shown in Table I.

On-chip bandgap references for biasing would improve the integration of the current driver in building multiple channel EIT systems. Additionally, a future iteration would require careful placement of the output port, so that it is sufficiently isolated from adjacent signals to reduce the parasitics.

VI. CONCLUSION

A CMOS current driver based on current conveyor architecture has been presented. The design was fabricated in the 0.18-μm process and can deliver 1.2mA of current up to frequencies of 10MHz. The above performance is achieved while mainting harmonic distortion of less than 1%. The current driver performance has been measured using a custom built PCB. The circuit is intended for use in active electrodes and EIT applications which require high frequency of operation to detect cancerous tissues.

REFERENCES

[1] G. Saulnier, R. Blue, J. Newell, D. Isaacson, and P. Edic, "Electrical impedance tomography," *IEEE Signal Processing Magazine*, vol. 18, no. 6, pp. 31–43, 2001.

[2] A. S. Tucker, R. M. Fox, and R. J. Sadleir, "Biocompatible, High Precision, Wideband, Improved Howland Current Source With Lead-Lag Compensation," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, pp. 63–70, feb 2013.

[3] L. Yan, J. Bae, S. Lee, T. Roh, K. Song, and H.-J. Yoo, "A 3.9 mW 25-Electrode Reconfigured Sensor for Wearable Cardiac Monitoring System," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 353–364, jan 2011.

[4] L. Constantinou, I. F. Triantis, R. Bayford, and A. Demosthenous, "High-Power CMOS Current Driver With Accurate Transconductance for Electrical Impedance Tomography," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, pp. 575–583, aug 2014.

[5] L. Constantinou, R. Bayford, and A. Demosthenous, "A Wideband Low-Distortion CMOS Current Driver for Tissue Impedance Analysis," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, pp. 154–158, feb 2015.

[6] S. Hong, J. Lee, J. Bae, and H.-J. Yoo, "A 10.4 mW Electrical Impedance Tomography SoC for Portable Real-Time Lung Ventilation Monitoring System," *IEEE Journal of Solid-State Circuits*, vol. 50, pp. 2501–2512, nov 2015.

[7] J. Jossinet, "The impedivity of freshly excised human breast tissue," *Physiological Measurement*, vol. 19, pp. 61–75, feb 1998.

[8] R. Halter, A. Hartov, and K. Paulsen, "A Broadband High-Frequency Electrical Impedance Tomography System for Breast Imaging," *IEEE Transactions on Biomedical Engineering*, vol. 55, pp. 650–659, feb 2008.

[9] V. Saxena and R. Baker, "Indirect feedback compensation of CMOS op-amps," in *2006 IEEE Workshop on Microelectronics and Electron Devices, 2006. WMED '06.*, pp. 3–4, IEEE.

[10] B. Wilson, "Recent developments in current conveyors and current-mode circuits," *IEE Proceedings G Circuits, Devices and Systems*, vol. 137, no. 2, p. 63, 1990.

[11] A. Sedra and K. Smith, "A second-generation current conveyor and its applications," *IEEE Transactions on Circuit Theory*, vol. 17, pp. 132–134, feb 1970.

[12] I. Jivet and B. Dragoi, "On-electrode autonomous current generator for multi-frequency EIT," *Physiological Measurement*, vol. 29, pp. S193–S201, jun 2008.

[13] A. Sedra, G. Roberts, and F. Gohh, "The current conveyor: history, progress and new results," *IEE Proceedings G Circuits, Devices and Systems*, vol. 137, no. 2, p. 78, 1990.

[14] E. Sackinger and W. Guggenbuhl, "A high-swing, high-impedance MOS cascode circuit," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 1, pp. 289–298, 1990.

[15] A. Zeki and H. Kuntman, "Accurate and high output impedance current mirror suitable for CMOS current output stages," *Electronics Letters*, vol. 33, no. 12, p. 1042, 1997.

[16] R. J. Baker, Institute of Electrical and Electronics Engineers., and IEEE Solid-State Circuits Society., *CMOS : circuit design, layout, and simulation*. 2008.

[17] T. C. Carusone, D. Johns, K. W. K. W. Martin, and D. Johns, *Analog integrated circuit design*. John Wiley & Sons, 2012.

[18] "Analog/Mixed-Signal Semiconductor Foundry: XH018," *https://www.xfab.com/technology/cmos/018-um-xh018/*.

[19] R. Cook, G. Saulnier, D. Gisser, J. Goble, J. Newell, and D. Isaacson, "ACT3: a high-speed, high-precision electrical impedance tomograph," *IEEE Transactions on Biomedical Engineering*, vol. 41, pp. 713–722, aug 1994.