A 1 MHz Miniaturized Electrical Impedance Tomography System for Prostate Imaging

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***Abstract*—An ASIC for a high frequency electrical impedance tomography (EIT) imaging system for prostate cancer screening is presented. The ASIC enables a small form-factor architecture, which ensures high signal-to-noise ratio (SNR) at MHz frequencies. The 4-channel ASIC was designed and fabricated in a standard CMOS 0.18-μm technology and integrates a novel current driver for current stimulus, instrumentation amplifier to interface with the tissue, VGA to provide variable gain and ADC with SPI interface for digitization. A prototype miniaturized EIT system was built and it was evaluated using a model transrectal imaging probe immersed into a tank filled with saline and a metal inclusion that demonstrated the open-domain problem of imaging prostate cancer lesion. The system maintained an SNR between 66 dB and 76 dB over the frequency range of 500 Hz to 1 MHz. Also, it produced reconstructed EIT images that depicted the presence of the small metal inclusion that modeled a prostate cancer imaging application.**

***Index Terms*—Electrical impedance tomography, EIT, application specific integrated circuit, ASIC, biomedical instrumentation, imaging, hardware system design, prostate imaging.**

I. Introduction

Standard prostate cancer screening is poor at gauging disease extent and aggressiveness. This often leads to overtreatment and unnecessary radical prostatectomy [1]. To improve prostate cancer screening, we and others have proposed transrectal electrical impedance tomography [2]. Transrectal EIT, or TREIT, is an imaging technique that distinguishes cancerous from benign tissue by identifying anomalies in the electrical properties of the prostate.

The challenge is that the best contrasts in TREIT are only observed for high-frequency ($\geq$ 100 kHz) impedance signatures [3]. Our recent TREIT system operates at these frequencies, but it is physically large; using it in an in-vivo clinical setting would require long cables to transmit analog signals between the probe and the instrumentation electronics [4]. And for high frequency analog signals, long cables are prone to channel cross talk and parasitic impedances, which severely degrade image quality [5].

If the EIT instrumentation analog front end (AFE) were built as an application specific integrated circuit (ASIC) and incorporated into the TREIT probe, it would reduce analog cable lengths from several meters to a few tens of centimeters. However, no ASIC-based system to date has met the technical specifications necessary for TREIT imaging. In this paper, we derive the performance requirements of a TREIT ASIC. We present a pathfinder ASIC for achieving these specifications, and we evaluate its performance in a prototype TREIT imaging system which requires high SNR, high frequency interrogation of an open-domain geometry.

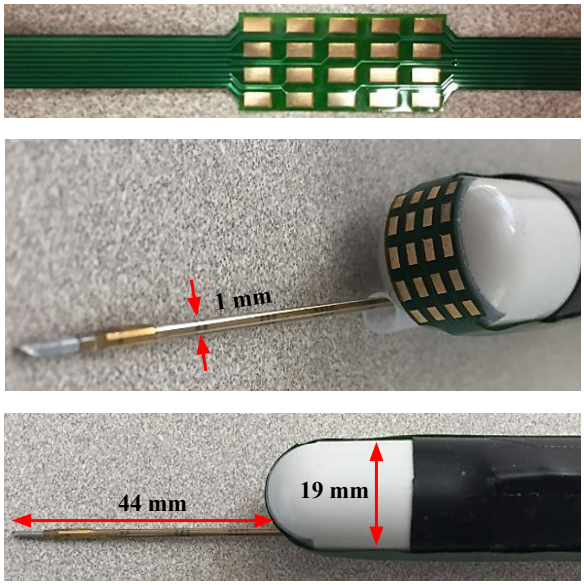


Fig. 1. Proposed TREIT probe for prostate electrical impedance tomography imaging. It comprises a flexible sonolucent PCB with a 4x5 grid array of electrodes (top) wrapped around an end-fired transrectal ultrasound probe with a biopsy needle (center and bottom).

II. Transrectal Electrical Impedance Tomography

We have designed and constructed a flexible sonolucent electrode array to interface with an end-fired transrectal ultrasound (TRUS) probe and a multi-electrode biopsy needle, able to simultaneously sense electrical signals and extract tissue cores (see Fig. 1). During biopsy, the electrodes are used to inject low amplitude sinusoidal currents into the tissue, and then used to read the resulting boundary voltages that develop on the surface of the tissue. The voltage difference between a pair of electrodes due to a particular current source/sink configuration is known as an IIVV pattern. In Fig. 2 for instance, IIVV pattern 1-15-16-14 is the voltage difference between electrodes E16 and E14 when current is injected into E1 and sunk by E15. Hundreds of these IIVV patterns are collected and used to reconstruct a single tomography-like map of conductivity and permittivity of prostatic tissue.

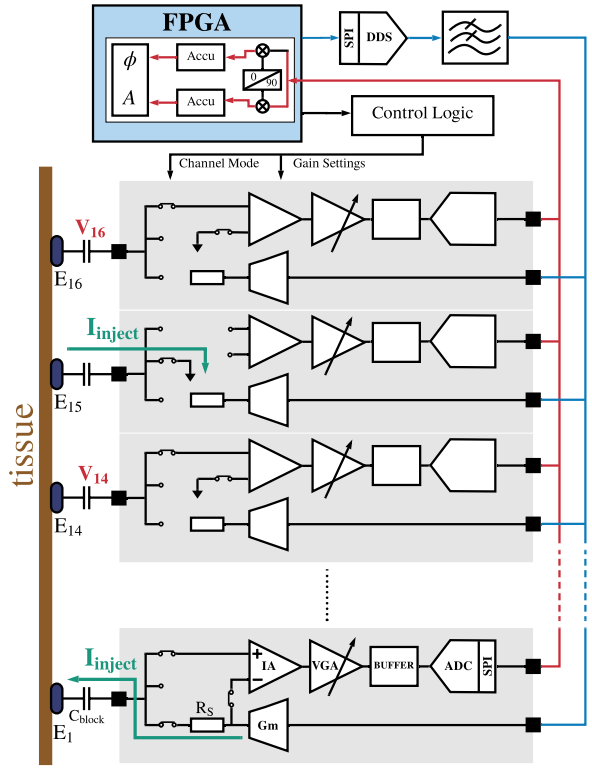


Fig. 2. Block diagram of a the designed 16-electrode EIT system. AC current excitation is performed using a pair of electrodes (1 and 15) and the voltages induced on the remaining electrodes are measured. DC isolation between the patient and instrumentation is achieved using capacitor, C_{block}. The DC blocking capacitor is a discrete component, placed off-chip with a value of 1μF.

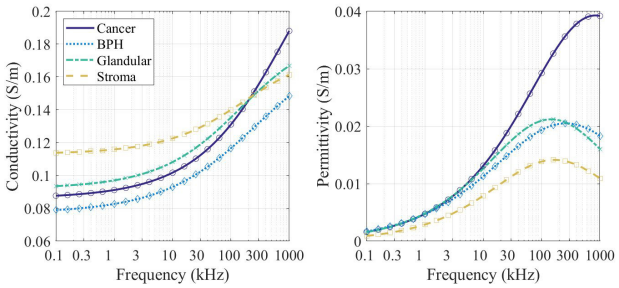


Fig. 3. The conductivity and permittivity of prostate tissue from 100 Hz to 1 MHz. In the graph legend 'Cancer', 'BPH', 'Glandular', 'Stroma' represent prostate adenocarcinoma, benign prostatic hyperplasia, nonhyperplastic glandular tissue, and stroma respectively. Cancerous tissues exhibit significantly lower conductivity, whereas the admittivity between cancerous and surrounding tissues increase with higher frequency of operation [3].

III. EIT Specifications to Detect Cancer

A. Operating Frequency

As we showed in previous work with ex-vivo samples, the admittivity properties of the prostate are higher in malignant than in benign tissue [3]. Also, the difference in admittivity values is most pronounced for frequencies above 100 kHz (Fig. 3). To make use of this high contrast region, we require that the ASIC current driver and voltage readout chain operate up to at least 1 MHz.

B. Signal-to-Noise Ratio

For the TREIT image to be clinically useful, the IIVV patterns must be measured with adequate signal-to-noise ratio (SNR). In particular, the SNR of the amplitude and phase of boundary voltage measurements (like V_{14} and V_{16} in Fig. 2) must be sufficiently high.

We estimated the minimum required SNR by simulating a 3D finite element method (FEM) model of the prostate and an end-fired 20 electrode TREIT probe [6](see Fig. 4). To detect a 5 mm cancerous lesion that is 4 mm away from the TREIT probe, the SNR of the difference in IIVV patterns between the cancerous tissue and a normal, 'reference' prostate must be at least 10 dB. That is,

$$\mathrm{SNR}_{\Delta_{vv}} = 10\log_{10}\left(\frac{\overline{V_c}^2}{\sigma_{vv}^2} - \frac{\overline{V_{ref}}^2}{\sigma_{vv}^2}\right) \geq 10\mathrm{dB}, \qquad (1)$$

where V_c is the IIVV pattern for the prostate with the lesion, and V_{ref} is the same IIVV pattern for a reference healthy prostate. The overbars denote the mean of these voltages, taken over several repeated measurements in a real-world, noisy environment. Also, σ_{vv} is their standard deviation.

We used the FEM model to generate an exhaustive set of (noise-free) IIVV patterns from 100 Hz to 1 MHz, with and without a lesion. For each pattern, we set $\mathrm{SNR}_{\Delta_{vv}} = 10$ dB and solved Eqn. 1 for σ_{vv}. From this, we derived the minimum allowable SNR for boundary voltage measurements. Figure 5 shows that this SNR is 65-90 dB for the phase component and approximately 80 dB for the amplitude component. When we perform the FEM simulation with electrodes on the biopsy needle (versus on the TREIT probe), we find the single-ended voltage SNR requirements can be relaxed to 55-73 dB. This is because the biopsy needle is placed inside the prostate, and is closer to typical cancerous lesions found in the prostate (see Fig. 4 [2]).

C. Input voltage range

Generally for an M-electrode EIT system, we need at least M*(M-3)/2 IIVV measurements with the prescribed level of signal-to-noise ratio in order to reconstruct a useful image. However, depending on the tissue properties, current injection pattern and current injection amplitude, the system could encounter some boundary voltages that are too small to be practicably measured with the required level of SNR. We can discard these low-amplitude measurements, as long as there are enough other remaining measurements for image reconstruction. From our FEM simulations, we found that discarding boundary voltages smaller than 30 mV still leaves us with several hundred IIVV patterns – enough to perform image reconstruction in a 20 electrode system. Also, given the maximum safe current injection limits [7], the largest expected

amplitude for the boundary voltage is 1 V. So, the EIT system is required to handle boundary voltages with an amplitude dynamic range of 30 mV to 1 V.

D. Other Considerations

For patient comfort, and to minimize motion artifact, the TREIT frame rate should be at least 10 frames per second (FPS). This means that the system must measure all of the required IIVV patterns, and complete the image reconstruction algorithm, in 100 ms or less.

Accuracy and linearity requirements are less stringently defined, especially with the use of our calibration techniques (See Appendix A). Still, it is typical to design for $\geq 99\%$ accuracy and ≤ -40 dB total harmonic distortion [8], [9], [10].

IV. Analog Front-End ASIC

We designed an instrumentation analog front end ASIC to meet the above system-level specifications. Figure 6 shows the schematic of one channel of our custom IC, while the chip microphotograph of the ASIC, fabricated in the X-Fab 0.18-μm CMOS process, is shown in Fig. 7. It is a modified, 4-channel version of our previously-introduced EIT analog front end circuitry (AFE) [11], [12], [13]. As Fig. 6 shows, the AFE comprises an instrumentation amplifier for amplifying electrode voltage differences, a variable gain amplifier to accommodate the 30 mV to 1 V input voltage range, a unity gain buffer ADC driver, and a 10-bit successive-approximation register (SAR) ADC. Figure 8 shows the measured channel cross-talk from a sample ASIC. The differences in cross talk are due to slight asymmetries in channel placement and their surrounding circuitry. To avoid cross-channel interference, pad isolation is achieved with a combination of physical distance and the use of separate ground rails for the analog and digital circuits.

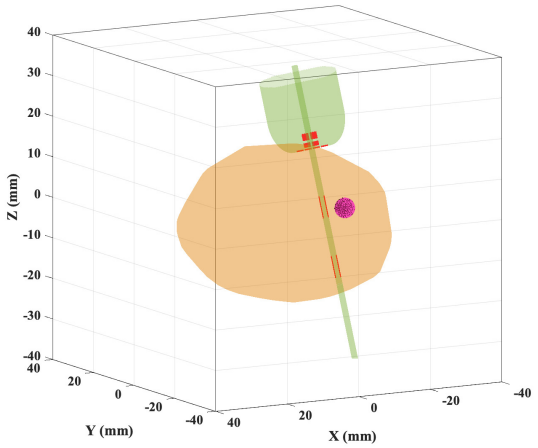


Fig. 4. Simulation setup for determining the SNR requirements of amplitude and phase for boundary voltage measurements. Prostate (orange), transrectal ultrasound (TRUS) and biopsy needle (green), and tumor (magenta). The FEM uses conductivity and permittivity values based on reported ex-vivo prostate tissue [3].

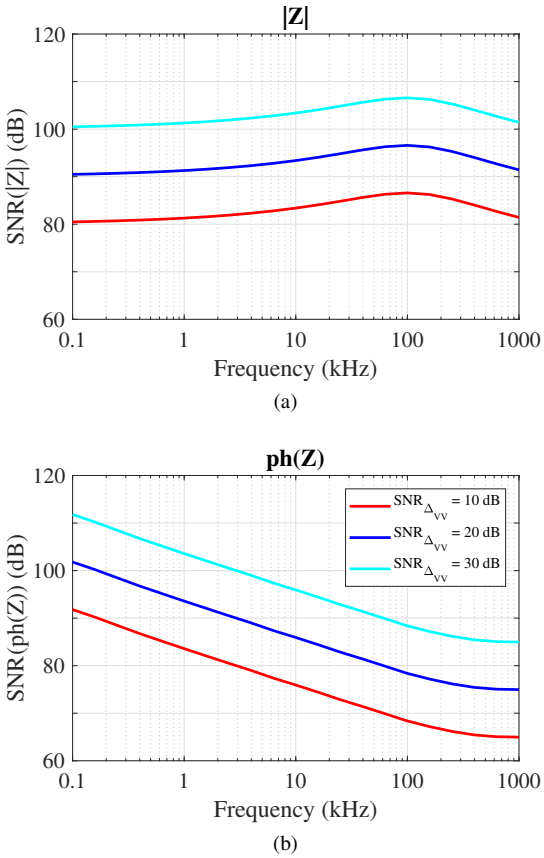


Fig. 5. The absolute measurement SNR required to achieve difference SNR (i.e. $\mathrm{SNR}_{\Delta_{VV}}$) values of 10 dB, 20 dB and 30 dB. The curves were produced using the FEM simulations and setup shown in Fig. 4. (a) Amplitude SNR (b) Phase SNR.

A. Current Driver

We used the current conveyor (CCII)-based current driver shown in Fig. 9 to inject sinusoidal currents of up to 1 $\mathrm{mA_{pp}}$ into the tissue under study. As Fig. 9 (a) shows, the current driver's input voltage, $\mathrm{V_Y}$, is produced by an off-chip direct digital synthesis (DDS) block and is buffered to $\mathrm{V_X}$, which generates a current $\mathrm{I_X} = \frac{\mathrm{V_X}}{\mathrm{R_X}}$ through resistor $\mathrm{R_X}$. The CCII mirrors this current to the output, $\mathrm{I_Z} = \mathrm{I_X}$, driving it through a DC-blocking capacitor, $\mathrm{C_{block}}$ and into the tissue. $\mathrm{C_{block}} = 1\mu\mathrm{F}$, protects the patient from DC currents, without the physical bulk of a transformer Since the resistor $\mathrm{R_X}$ provides a linear voltage-to-current conversion, the output current exhibits a relatively low THD of 0.15% for a 1 MHz, 1 $\mathrm{mA_{pp}}$ output. The servo loop shown in Fig. 9 (b) is necessary to maintain an appropriate DC bias voltage at the current driver's output. The operational transconductance amplifier (OTA) in the servo loop holds the output node fixed at $\mathrm{V_{CM}}$; ideally the feedback is active only at DC, due to the integrating action of a large external capacitor, $\mathrm{C_{EXT}}$. Finally, the current driver has a gain-boosted cascode output stage (see Fig. 9 (c))[14], [15] which provides an output impedance of 0.1 MΩ at 1 MHz. The 0.1 MΩ output impedance of the current driver is still significantly higher than that of the tissue impedance, which is 145 Ω at this frequency [12].

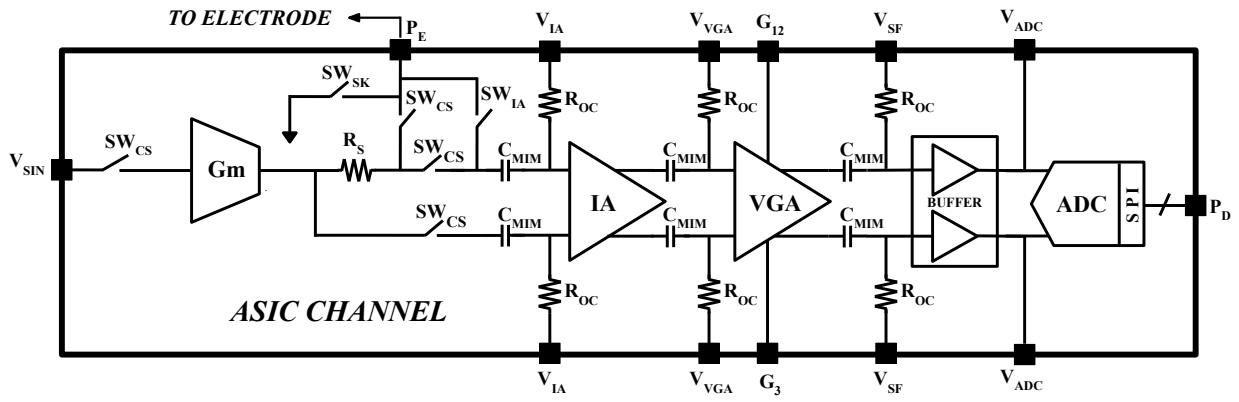


Fig. 6. Details of one channel of the 4-channel EIT instrumentation AFE ASIC. The on-chip switches are used to configure the channel in a current-source, current-sink or voltage-read mode. On-chip capacitors decouple each stage and resistors implemented as off-state transistors are used for input biasing. The IA, VGA, buffer and the ADC form the voltage readout chain [11]. The digital data from the ADC is sent off-chip using a SPI interface to compute amplitude and phase with a matched filter on a FPGA. The V_{SIN} pad is for the sinusoidal input to the current driver, P_E for the electrode connection, and P_D for the digital data to be sent off-chip. The remaining pads are used for biasing internal circuits of the readout chain. The performance of the 4-channel ASIC was measured using a custom built PCB.

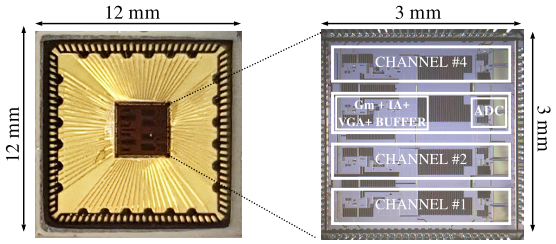


Fig. 7. Chip Microphotograph. 4 channels are integrated into a single ASIC. Various blocks are shown. The packaged chip measures 12 mm x 12 mm and the die size is 3 mm x 3 mm.

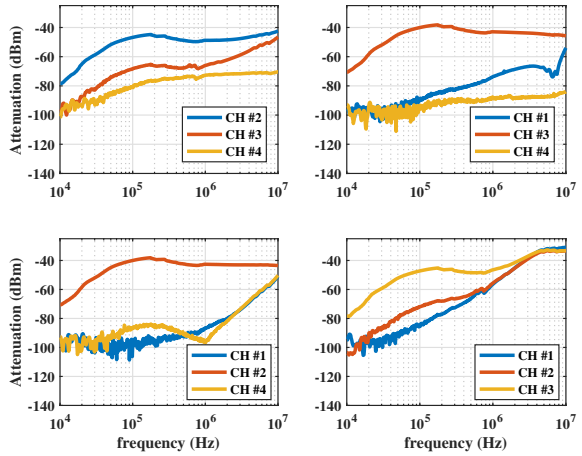


Fig. 8. Channel cross-talk for all channels on the 4-channel ASIC. Each channel is driven with a sinusoid (power of 0 dBm) and the fundamental magnitude appearing at the output of the VGA (with channel gain of 3 V/V) on the remaining channels measured with respect to the driven channel. A spectrum analyzer with a tracking generator is used for this measurement, for frequency range of 10 kHz to 10 MHz.

B. Readout Chain

When current is injected into the tissue, the readout chain of Fig. 6 is used to amplify, sample and digitize the sinusoidal voltage that develops on the tissue surface. Each voltage reading involves multiple samples (or "taps"), from which the FPGA-implemented digital matched filter extracts the sinusoidal voltage's amplitude and phase. To ensure successful EIT image reconstruction, the extracted amplitude and phase must be measured with an SNR of at least 65 dB. To achieve this, we considered the readout chain's thermal noise, quantization noise and number of taps per measurement, which all factor into the SNR via [16],

$$\mathrm{SNR_A} = 10 \cdot \log_{10} \cdot \left[\frac{\mathrm{A}^2 (\frac{\mathrm{N_{tap}}}{2})}{\left(\frac{\mathrm{V_{FS}}}{2^{\mathrm{B}}}\right)^2 \cdot \frac{1}{12} + \sigma_{\mathrm{n}}^2} \right] \tag{2}$$

where A is the maximum expected voltage amplitude, and $\mathrm{N_{tap}}$ is the number of taps (or samples) in the matched filter. Also, $\left(\frac{\mathrm{V_{FS}}}{2^{\mathrm{B}}}\right)^2 \cdot \frac{1}{12}$ is the quantization noise power, where B is the ADC resolution and σ_{n} is the standard deviation of the thermal noise referred to the ADC input.

The instrumentation amplifier and variable gain amplifier cascade produces the majority of the thermal noise, on the order of $\sigma_{\mathrm{n}} = 1\ \mathrm{mV_{rms}}$. Meanwhile, the ADC resolution is ideally $\mathrm{B} = 10$ bits to maximize power efficiency [11], [17], [18]. Assuming a maximum voltage amplitude of $\mathrm{A} = 1$ V , a full scale voltage of $\mathrm{V_{FS}} = 1.2$V, and a minimum system SNR of 70 dB, this gives the required number of taps per voltage measurement as,

$$\mathrm{N_{tap}} \geq \frac{2 \cdot 10^{\frac{\mathrm{SNR_A}}{10}}}{\mathrm{A}^2} \cdot \left(\left(\frac{\mathrm{V_{FS}}}{2^{\mathrm{B}}}\right)^2 \cdot \frac{1}{12} + \sigma_{\mathrm{n}}^2 \right)$$

$$\mathrm{N_{tap}} \geq 22$$

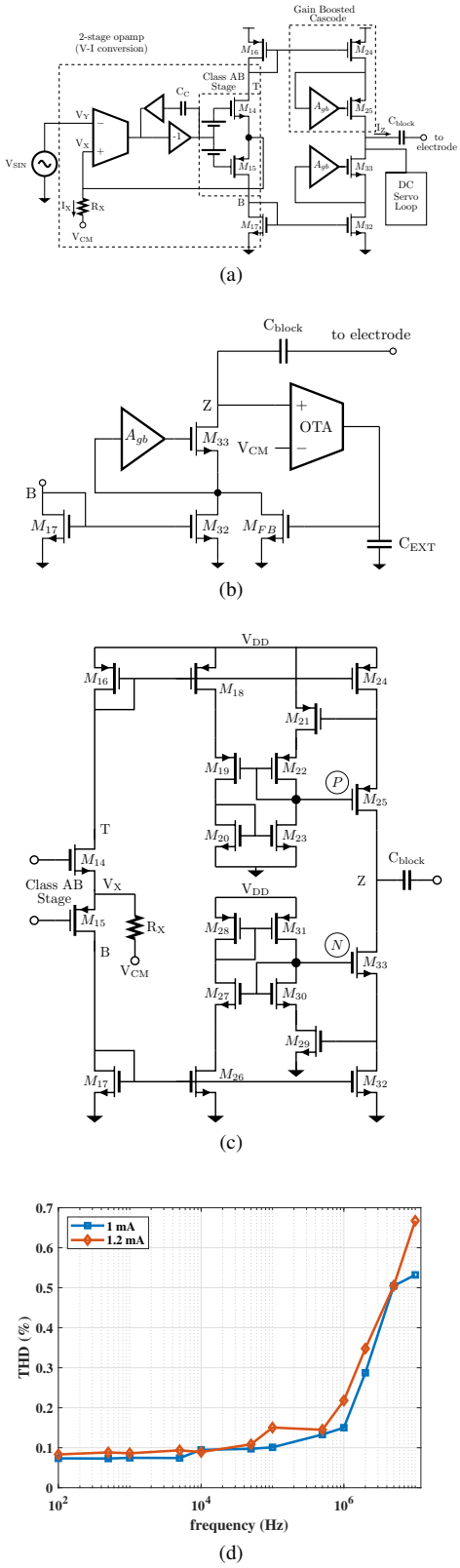


Fig. 9. (a) Current conveyor II (CCII) based wide-band current driver [12]. (b) Structure designed to keep the current driver in the proper operating regime. (c) The high output impedance is achieved using a gain enhanced cascode structure. (d) Plot of total harmonic distortion for the current driver across frequencies for 2 current levels.

We chose $N_{tap} = 100$, which allows for some margin of error. To meet the 10 fps frame rate, the voltage measurements must be taken for all possible current injection patterns ($\frac{16*15}{2} = 120$ patterns for a 16 electrode system) in less than 0.1 seconds. Since we need 100 taps per measurement to meet the SNR specification, this translates to an ADC sample rate of at least $\frac{100*120}{0.1} = 120,000$ samples per second. We designed the ADC for 250 kSa/s to allow for settling time between current injection patterns. To process signals higher than 125 kHz, we used the undersampling technique described below. The measured SNR across frequencies and the readout chain details are shown in Fig. 10.

As Figs. 10 (a) and (b) show, our instrumentation amplifier and variable gain amplifier are based on the CCII architecture, which provides a high common-mode rejection ratio and high speed operation. The variable gain amplifier includes a resistive ladder in the input transconductance stage, allowing it to provide a range of gains from 0 dB to 21 dB. The readout chain performance was tested by measuring phantom loads that were soldered physically close to the chip. The measured ADC resolution was 8.84 bits, the thermal noise (referred to the ADC input) was $\sigma_n = 0.4\ mV_{rms}$, and the largest measured voltage amplitude was A = 0.6V [11]. So, the SNR predicted from Eqn. 2 is 74 dB, which closely matches the measured SNR results shown in Fig. 10(c).

C. Undersampling

Undersampling refers to sampling a signal at a rate lower than the Nyquist sample rate. This causes aliasing, a generally undesirable phenomenon because high frequency content can get superimposed onto low frequency content. In the case of undersampling an EIT boundary voltage, the effect of aliasing is simply to downconvert a high frequency sinusoid to a lower frequency. Other than additive thermal and 1/f noise, there is no low frequency content to interact with and distort the aliased signal. And, importantly for image reconstruction, aliasing preserves the original phase and amplitude of the boundary voltage.

For the undersampling technique to work well in practice, two constraints must be met. First, the sampling frequency and the input signal frequency must be coprime. This avoids the potential for repeated sampling of the same point (e.g. if a 1000 kHz signal were sampled at 100 samples/second, it is possible that only the zero crossings of the signal would be sampled). The second constraint is that there must be a whole number of samples in one period of the aliased signal. This enables a proper matched filter implementation following the ADC, thus maximizing the SNR of the readout chain.

Considering the two constraints above, there is significant overhead in designing an undersampling scheme for any arbitrary interrogation frequency. Instead, our approach is to choose a fixed set of interrogation frequencies that fall within the frequency range of interest and that satisfy the two undersampling constraints via,

$$f_{in} = \frac{(N_{tap} \cdot K \pm 1) \cdot f_S}{N_{tap}} \quad (3)$$

where $N_{tap} = 100$ is the number of samples (i.e. matched filter taps) and $f_S \leq 250$ kHz is the ADC sample rate.

For example, for $f_S = 100$ ksps, $N_{tap} = 100$, and $K = 10$, we have $f_{in} = 1001$ kHz. This gives an aliased signal of 1 kHz, for which we obtain 100 samples in one full period of 1 ms. The frequency domain representation for this example is shown in Fig. 11.

V. Measurement Results

We evaluated the performance of our ASIC-based multi-frequency EIT system with the modular test setup shown in Figs. 12 and 13. It is a 20-channel system, comprising 5 daughterboards (each housing a 4-channel instrumentation ASIC), an Adafruit Feather HUZZAH (Adafruit Industries, New York, NY) for wireless data transmission and an Artix-7 FPGA evaluation board (Xilinx Inc., San Jose, CA) for system control and match-filter amplitude/phase extraction. A single motherboard provides power and I/O slots to host all of the above components. This modular approach facilitates testing and debugging. For example, one of the daughter boards was sacrificed and used to monitor the FPGA's communication and control signals, leaving 16 fully-functional channels for image reconstruction experiments. Following this proof of concept system, we will build future versions on a single PCB for a hand-held form factor.

In addition to an instrumentation ASIC, each daughter board (see Fig. 14) contains one AD9834 sinusoidal waveform generator chip (Analog Devices Inc., Norwood, MA) to provide input to the ASIC's current drivers. The waveform generator's output frequency and amplitude are set by the FPGA via SPI. The FPGA also uses SPI to communicate with the instrumentation ASICs: to set the channels' readout gain, operation mode (current sink, current source or voltage readout) and to collect the digitized voltages. In turn, initial setup information (number of electrodes, vector of injection frequencies, etc.) is

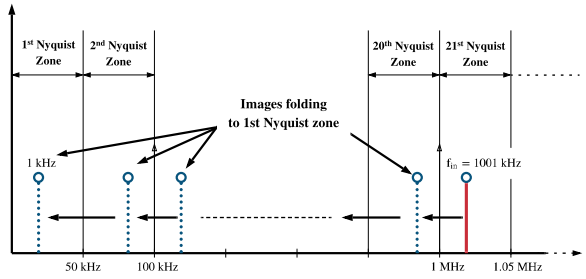
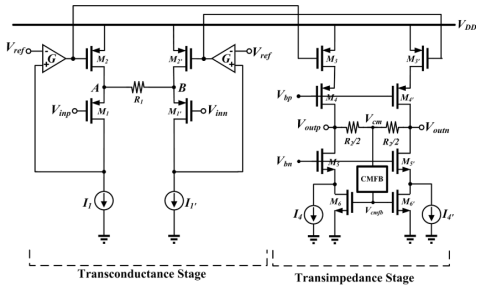
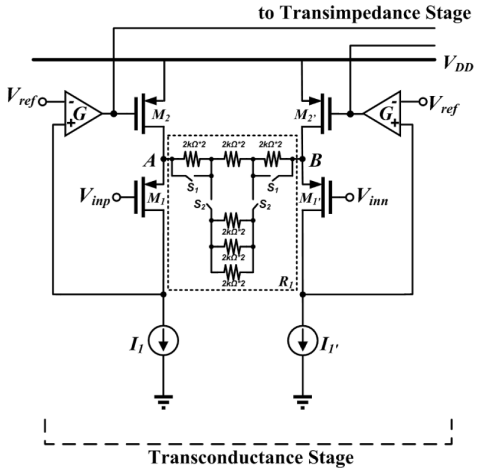


Fig. 11. Frequency domain representation for interrogation frequency of 1001 kHz and 100 ksps sampling rate. The aliased frequency is folded back to the 1st Nyquist zone representing a 1 kHz signal. 100 samples are obtained in a single waveform period of the aliased frequency.



(a)



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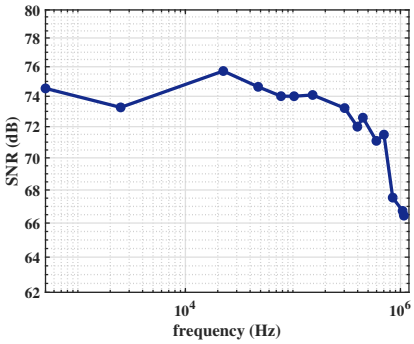

(c)

Fig. 10. (a), (b) Schematic of the IA and VGA [13]. (c) SNR plot across frequencies for the readout chain. The drop in SNR is due to the limited full power bandwidth of the ADC.

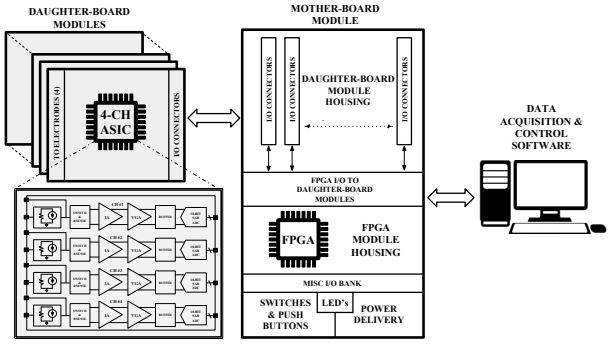

Fig. 12. Architecture of the 16-electrode channel EIT system. The custom built 4-channel ASIC implements the core EIT functionality and is included on a daughter-board module with required power, voltage references, current biases and switch IC's. A motherboard houses the daughter-board module and FPGA carrier board. The Artix-7 FPGA on the mother-board is responsible for control, data acquisition, and computations. The data from the FPGA is sent to the MATLAB software on the computer to form impedance matrices and re-construct images.

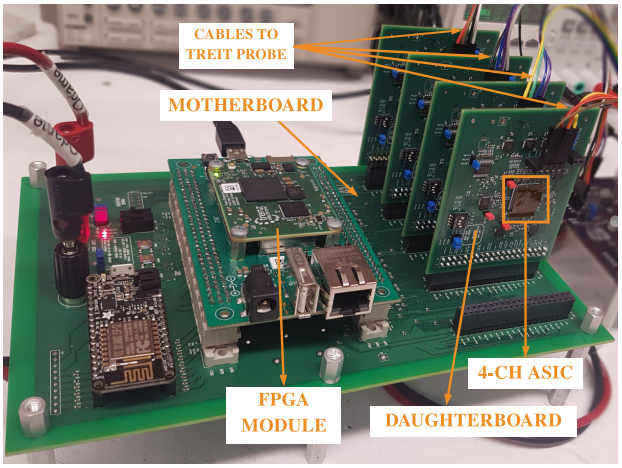

Fig. 13. 16-electrode EIT system for prostate imaging. A 4-channel ASIC resides on each daughter-board. Cables from daughter-boards connect to the saline tank or TREIT probe setups shown in Figs 15 and 18 respectively. The length of the cable from the instrumentation to the test setup is $\sim$ 30 cm. The system can be configured for a maximum of 20-electrodes for measurements.

downloaded to the FPGA from a workstation computer via UART.

A. Saline Tank Measurements

To validate the functioning of the EIT system, we performed impedance imaging experiments of a saline tank. An 8.5 cm diameter tank was filled to a height of 1.27 cm with a saline solution of conductivity 1000 μS/cm. The tank was fitted with

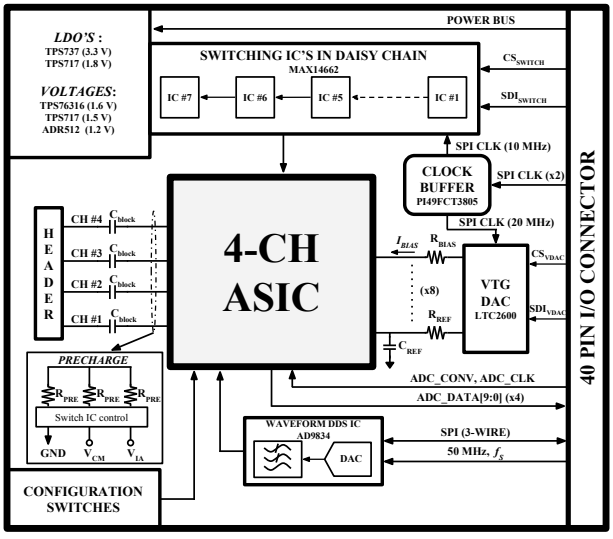

Fig. 14. Daughter-board module block diagram. The module includes the 4-channel ASIC which provides majority of the EIT functionality. Peripheral IC's generate voltage references, bias currents, sinusoidal stimulus for the ASIC and switching mechanisms for channel configuration. Several SPI interfaces are implemented to communicate with the IC's and the ASIC. Pre-charge circuits reduce settling time at the output of each channel. The channel outputs are connected to headers, using a DC blocking capacitor C_{block}. Power is supplied to each module from the I/O connectors. A large number of GND pins are included in the connectors to ensure proper ground connection with the motherboard.

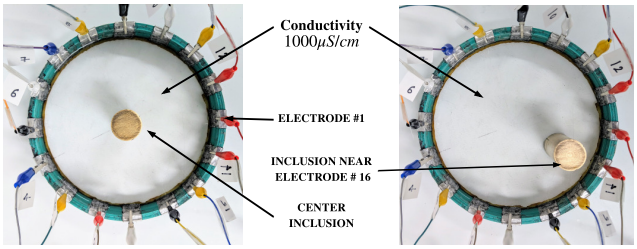

Fig. 15. Saline tank experiment setup with a 16-electrode EIT system. The conductivity of the solution was set to 1000 $\mu S/cm$. Brass rod inclusion at the center of the saline tank and inclusion placed close to electrode # 16.

conductive electrodes in contact with alligator clips attached to the tank. The spacing between each electrode was 3.25 cm. In an initial experiment, we took baseline measurements with only saline solution in the tank. Subsequent experiments involved a brass rod inclusion of diameter 1.3 cm placed inside the tank of saline solution: for one experiment, the rod was placed at the center of the tank; in another experiment, the rod was placed close to the edge, near electrode 16. The experimental setups with center and off-center inclusion is shown in Fig. 15. For each experiment, data was acquired for 6 frequencies from 1 kHz to 1 MHz with 240 current source/sink patterns per frequency and a current injection amplitude of 550 μA. The acquisition time is 38 ms per frame with a properly-compensated current driver. At the time of experimentation, our setup had slow settling behavior due to poor compensation and low phase margin (see Discussion section), leading to a measured acquisition time greater than 25 seconds.

We processed the data with our in-house reconstruction algorithm [19] to generate the impedance images shown in Figs. 16 and 17. Figures 16 and 17 represent difference images, so negative conductivities are possible, but the background should really result in a conductivity of zero, i.e. zero change from the reference set. Other than the 1 kHz results, the metal inclusion is clearly visible in image reconstructions. At 1 kHz, it is possible that the electrode-electrolyte interface is forming a double-layer capacitance. However, we are primarily interested in high frequency images from the system.

B. Transrectal Probe Experiment

To simulate the TREIT application, we tested our system with the probe and tank setup shown in Fig. 18. This experiment evaluated our system's ability to reconstruct images in an open-domain geometry, with no distal electrodes—this is a more challenging problem than the typical closed-domain EIT geometry, but it is necessary for the TREIT application.

The probe was a 3D-printed model of a Phillips C9 TRUS probe (Koninklijke Philips N.V., Amsterdam, Netherlands), around which was wrapped a flexible printed circuit board of 20 gold-plated electrodes. The probe was immersed in a saline tank solution of conductivity 1100 μS/cm. A tightly wound copper wire inclusion of diameter approximately 2 mm was placed at a distance of $\leq$ 1 mm from the probe tip (Fig. 19), to model a prostate cancer lesion. 16 of the probe electrodes

were connected to our EIT system 0.1 inch connectors. Data was acquired for 6 frequencies from 101 kHz to 1 MHz with 240 current source/sink patterns per frequency and a current injection amplitude of 235 μA. As the reconstructed images in Fig. 20 show, our EIT system was able to detect the metal inclusion (yellow blocks in the 3D images) across the various test frequencies.

C. Tumor Detection

The EIT system's ability to detect a tumor depends on the signal-to-noise ratio (SNR) of the boundary voltage measurements. As described in Section III-B, the SNR of the difference

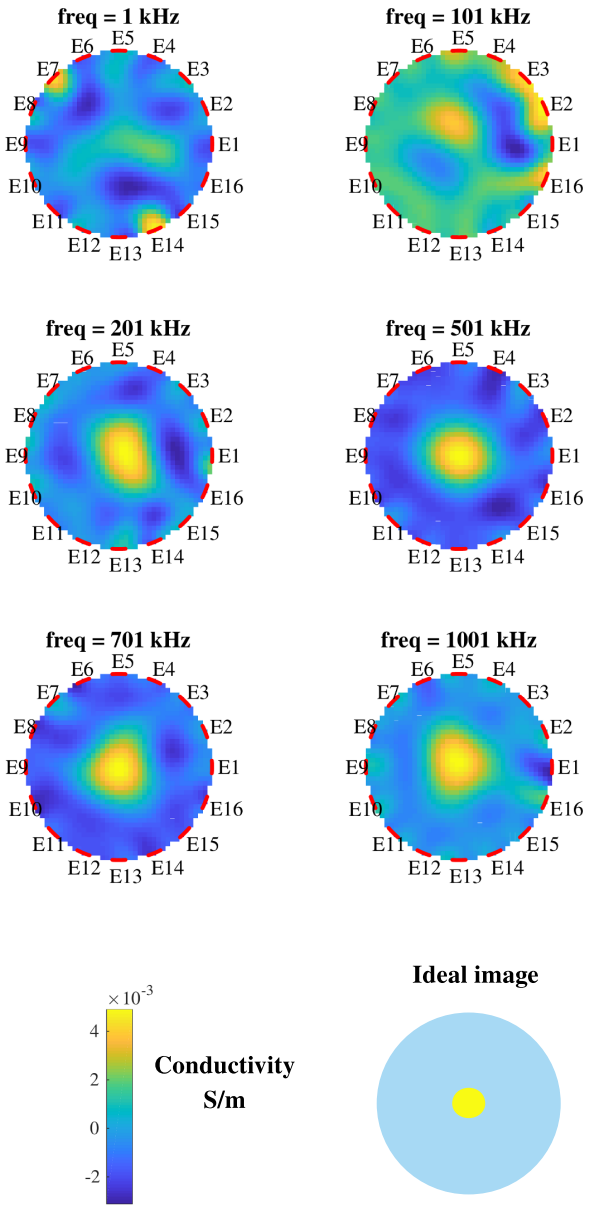

Fig. 16. Images obtained for the center inclusion with an ideal image to the left. Data for 1 kHz could not be obtained due to issues with hardware setup. It is included here as the images were obtained from the same dataset. Image reconstruction was performed using difference imaging and hence the conductivity scale does not represent the true values.

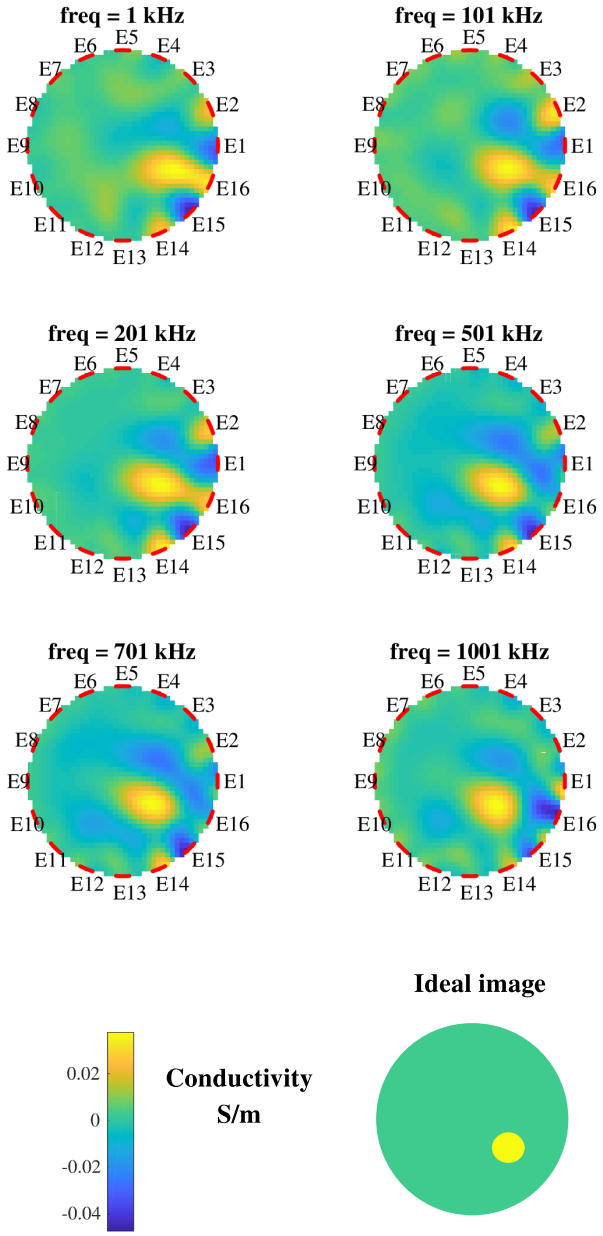

Fig. 17. Images obtained for the off-center inclusion with an ideal image to the left. All images obtained for the same dataset are shown. Image reconstruction was performed using difference imaging and hence the conductivity scale does not represent the true values.

in IIVV patterns between a normal, 'reference' prostate and one with a lesion must be 10 dB or better. That is, repeated from Eqn 1:

$$\mathrm{SNR}_{\Delta_{vv}} = 10\log_{10}\left(\frac{\overline{\mathrm{V_c}}^2}{\sigma_{vv}^2} - \frac{\overline{\mathrm{V_{ref}}}^2}{\sigma_{vv}^2}\right) \geq 10\mathrm{dB}, \qquad (4)$$

where $\mathrm{V_c}$ is the IIVV pattern for the prostate with the lesion, $\mathrm{V_{ref}}$ is the same IIVV pattern for a reference healthy prostate, and σ_{vv} is the rms noise of the boundary voltage measurements.

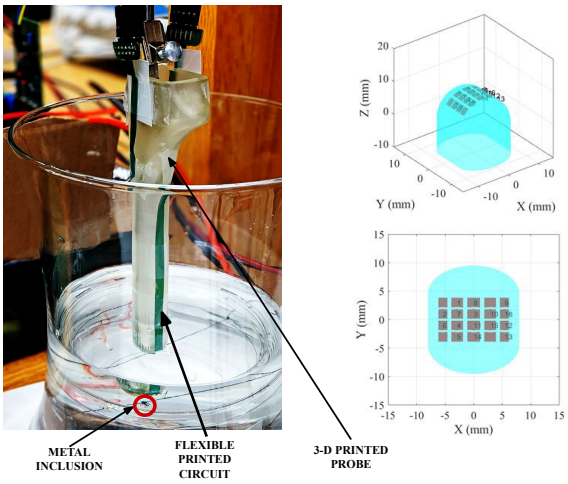

Fig. 18. TRUS setup with the electrode array on a flexible printed circuit, immersed in a saline tank solution.The 16 electrode positions used for our EIT measurements are shown in the bottom-right figure.

We estimated $\sigma_{vv} \approx 0.88$ mVrms by calculating the standard deviations of sets of 250 repeated measurements recorded from the TREIT experimental setup (Fig. 18). We also generated expected values for V_c and V_{ref} using the FEM simulation setup shown in Fig. 4. Finally, we combined the simulated V_c and V_{ref} values with the measured σ_{vv} values, to compute $SNR_{\Delta_{vv}}$ for an exhaustive set of IIVV patterns.

To detect a tumor, we need enough IIVV patterns with $SNR_{\Delta_{vv}}$ of 10 dB or better. From the Fig. 21 results, we conclude that our current EIT system can detect a range of tumor sizes, at a distance of 2 to 10 mm. Small tumor detection might be limited if we use only TRUS probe tip electrodes. But it is readily achievable if we include the biopsy needle electrodes, as predicted by our initial SNR calculations of Section III-B.

D. Position error

With the location of the inclusion at [-2 0 3] (dimensions in mm), assuming the center of the TRUS probe with electrodes as the origin, the mean reconstructed inclusion position was [-2.06, 0.34, 3.30] and the precision error across frequencies

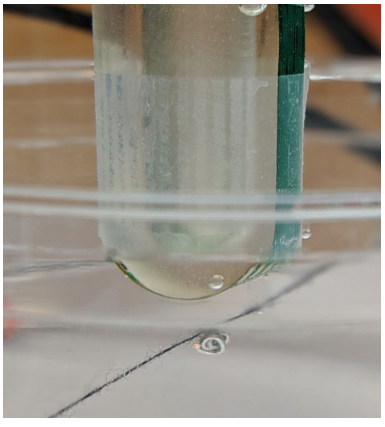

Fig. 19. Probe setup with a zoomed in section of the inclusion and separation from electrode array.

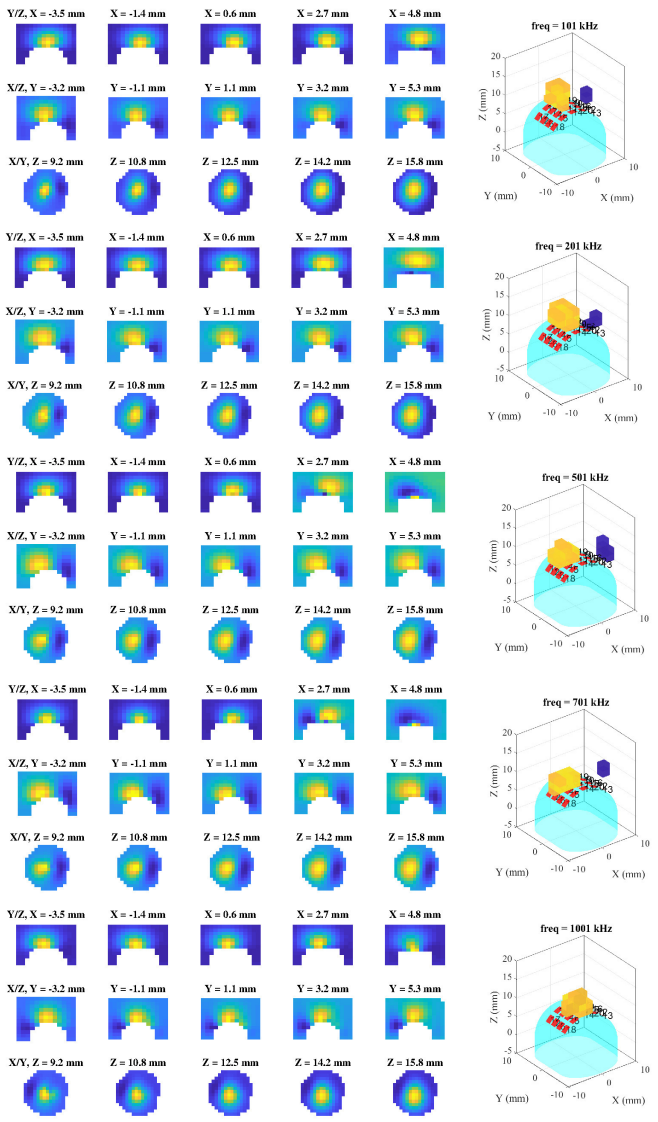

Fig. 20. Images obtained across frequencies for the 16-electrode TRUS setup in the saline tank shown in Fig. 18. The yellow blocks in the reconstructed 3D images are conductivity regions that are within 70 % of the maximum measured conductivity. That is, they represent the metal inclusion. The yellow and blue blocks are the result of a choice in thresholding. Reconstruction was done using difference imaging, so some sections appear to have a relatively high or a relatively low conductivity.

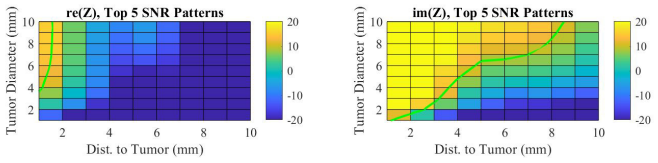

Fig. 21. $SNR_{\Delta_{vv}}$ for different values of tumor diameter and distance of electrodes from tumor, using the FEM simulation setup of Fig. 4 and measured noise values from TREIT experimental setup (Fig. 18). Data shown is for a 701 kHz interrogation frequency. The top 5 SNR patterns represents the selected IIVV patterns with the best SNR for the voltage measured at the electrodes. The light green line is the 10 dB contour as described by Eqn. 4.

TABLE I
EIT SYSTEM SPECIFICATIONS

Application		Prostate Imaging
ASIC		
Process		XFAB 0.18-μm CMOS
Supply Voltage	Analog	3.3 V
	Digital	1.8 V
Current Driver	Frequency	100 Hz - 10 MHz
	Amplitude	up to 1.2 mA
	Output Impedance	101 kΩ@ 1 MHz 19 kΩ@ 10 MHz
	THD	$<$ 1% @ 10 MHz
Read-out Chain	Gain	IA : 9.3 dB VGA : 0, 9.3, 21 dB
	Input Noise	IA : 14 nV/$\sqrt{\text{Hz}}$ VGA : 80, 27, 6.7 nV/$\sqrt{\text{Hz}}$
SAR ADC	ENOB	8.84 bits
	Sampling Rate	250 ksps (max)
Power (per channel)		11.4 mW
EIT System		
Electrodes		16
Scan Patterns		Programmable
THD (readout chain)		0.2% @ 1 MHz
Frequency		1 kHz - 1 MHz
SNR		66-76 dB
Digital Interfaces		SPI, UART

101 kHz to 1 MHz was 1.39 mm (standard dev = 0.21 mm).

VI. DISCUSSION

The performance specifications for our ASIC and overall EIT system are listed in Table I. In the context of transrectal electrical impedance tomography for enhancing prostate cancer diagnosis, the primary target specifications for an EIT analog front end are: 1 kHz to 1 MHz interrogation frequency range; 65-90 dB SNR (probe tip electrodes) or 55-73 dB SNR (biopsy needle electrodes); 16 to 20 electrode channels; 10 FPS data acquisition rate; hand-held form factor.

As Table II shows, existing EIT analog front ends that meet the measurement requirements were based on commercial-off-the-shelf (COTS) discrete components [4], [20]. So, with more than a dozen channels, these AFEs are too large to fit the hand-held form factor of a TREIT probe. This is crucial, because large instrumentation must be placed far from the patient, neccessitating long cables for transmitting analog signals between the electrodes and the rest of the EIT system. At high frequencies, this arrangement would severely degrade the system's SNR performance. ASIC-based AFEs address the problem of form factor, and can enable the high frequency interrogation required in a prostate imaging application.

Table II shows that our solution outperforms other ASIC-based AFEs in terms of high SNR at high frequencies. Our solution meets all the specifications for prostate imaging with the biopsy needle, while falling a little short for use with probe electrodes. The reduction in SNR for higher frequencies is due to some limitations of undersampling, including limited bandwidth of the ADC/ADC driver and the addition of (aliased) high frequency noise to low frequency noise. Nevertheless, our experimental results suggest that, even for the more stringent probe electrodes application, our EIT system is able to detect high-contrast small inclusions in a saline solution. An improved ADC with ENOB $\geq$ 10 would produce even better performance [18].

The frame rate of the system depends primarily on the ADC's sample rate and the amount of settling time needed between measurements. Our current driver exhibited poor phase margin, and unfortunately produced a long settling time. Referring to Fig. 9(b), the current driver has two dominant poles: one at $\frac{G_m}{C_{EXT}}$ rad/s due to the OTA and external capacitor of the servo loop, and another at $\frac{1}{(R_{out} \cdot C_{block})}$ rad/s, where R_{out} is the output impedance of the current driver. These poles are close in frequency and result in poor phase margin. This caused slow settling and the target frame rate was not achieved. The solution to this problem is to increase the frequency of the servo-loop pole; we have verified this solution in simulation and will implement it in future iterations of the chip.

VII. CONCLUSION

We derived the detailed system level specifications necessary for transrectal electrical impedance tomography. A 4-channel ASIC was designed and fabricated in the CMOS 0.18-μm technology for high frequency EIT. It integrates a novel current driver for current injection, instrumentation amplifier to interface with the tissue, VGA to provide variable gain and an ADC with SPI interface for digitization. The readout chain operates between 500 Hz - 1 MHz with an SNR range of 66 dB - 76 dB. The ASIC is integrated into a prototype modular 16-electrode EIT system consisting of daughter-boards, motherboard, FPGA and custom software framework. Saline tank experiments and transrectal probe setups were used to obtain reconstructed images of inclusions in a saline tank solution. The results in this paper demonstrate that our ASIC-based EIT system is able to perform high-frequency conductivity images from a transrectal probe appropriate for prostate imaging applications. This capability has never before been demonstrated in an ASIC-based EIT system, and it suggests a path forward for integrating EIT imaging into prostate biopsy procedures.

APPENDIX A
CALIBRATION

The designed EIT system is prone to various sources of systematic errors, particularly for the ASIC channel. Potential sources of errors are listed below and a pictorial representation is shown in Fig. 22.

- *AD9834 IC output :* The AD9834 IC provides the sinusoidal input for the current drivers on the ASIC for each daughter-board module. The differences in the

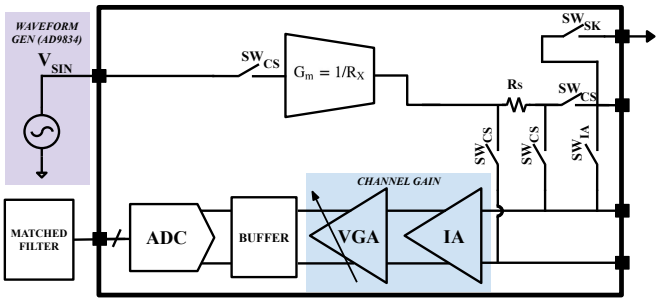

Fig. 22. Sources of measurement errors in the EIT system.

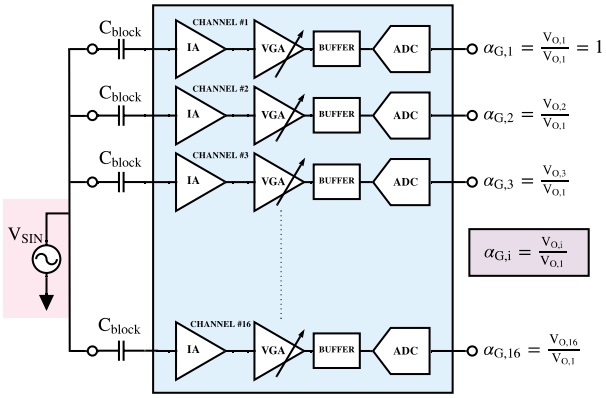

Fig. 23. Circuit to determine the calibration coefficient of the channel gain. All channels of the EIT system are configured in the voltage-read mode and input with a known voltage with amplitude A. With channel # 1 as the reference, and gain, G of the readout channels, the calibration coefficient, α_{G} is calculated for all channels.

output voltage amplitudes from the AD9834 IC across the modules need to be accounted for during calibration.

- *On-chip resistors :* Each ASIC channel includes 2 on-chip resistors: $\mathrm{R_X}$ for generating the current to be injected into the tissue, and $\mathrm{R_S}$ for sensing the current (see Figs. 9 and 6). Due to process variations during fabrication the resistor values vary. This causes variation in both the injected current and the voltage induced across the sense resistor. Variation in the resistor values should be included in the measurements.
- *Channel gain :* The readout chain consists of the IA with a fixed gain of 3 V/V, and VGA with variable gains of of 1, 3 and 12 V/V. Due to process variations there is a channel-to-channel variation in gain which affects the voltage measurements.

1) Voltage-read mode: A calibration scheme is proposed for the EIT system which includes all the above sources of errors. First, the measurement errors in the voltage-read mode is calculated and accounts for the channel variation due to IA and VGA gain. The circuit to calculate the gain calibration coefficient of each channel is shown in Fig. 23. All the channels of the EIT system are configured in the voltage-read mode and connected to a sinusoidal voltage source with known amplitude, A. Ideally the voltage at the output of each channel is,

$$\mathrm{V_O} = \mathrm{A} \cdot \mathrm{G} \tag{5}$$

where G is the gain of the readout chain for all channels in the EIT system. However, due to the variations in channel gain, the value of $\mathrm{V_O}$ varies across channels. A calibration coefficient, α_{G} is defined which accounts for the gain variation with channel # 1 as the reference. The calibration coefficient is given as,

$$\alpha_{\mathrm{G,i}} = \frac{\mathrm{V_{O,i}}}{\mathrm{V_{O,1}}} \ , \tag{6}$$

where i represents the channel number in the EIT system. The procedure for obtaining the coefficient, α_{G}, is repeated for all possible gain combinations of the readout chain across the desired frequencies.

2) Current-source mode: The circuit in Fig. 24 determines the calibration coefficients for the channel configured in the

TABLE II
PERFORMANCE COMPARISON OF EIT SYSTEMS

	Target	[20]	[4]	[21]	[22]	This Work
AFE form factor	ASIC	Multiple COTS	Multiple COTS	ASIC	ASIC	ASIC
Frequency (kHz)	1-1000	10-1000	1-1000	45-1000	11	0.5-1000
SNR (dB)	65-90; 55-73	45-82	84-100	48-54	83	66-76
# Channels	16-20	32 (max 48)	16	16	16	16 (max 20)
Frame Rate (fps)	10	546	30	122	25	26[1]
Power (mW/channel)	–	N/A[2]	>100	250	>300	90

[1] Our hardware incorporated 4 ASIC's in the system to obtain a 16-electrode system. The theoretical frame rate value is based on using 96 ii-patterns and 250 kHz sampling frequency. The 26 fps value could not be achieved by our system due to the poor phase margin as explained in Section VI. A future iteration of the design will incorporate proper compensation techniques to achieve the theoretical frame rate.
[2] Not available.

current-source mode. The sources of error in this configuration are the output voltage amplitude differences from the AD9834 IC, on-chip resistor variations, and channel gain.

The on-chip resistor, R_X generates the sinusoidal current in the V-I conversion stage of the current driver. The current output from the current driver is,

$$I_Z = \frac{\alpha_{SIN} \cdot V_{SIN}}{\alpha_X \cdot R_X} \ , \tag{7}$$

where, I_Z is the output from the current driver, V_{SIN} is the output voltage amplitude from the waveform generator IC, α_{SIN} is the corresponding calibration coefficient, and α_X is the calibration coefficient of the on-chip resistor, R_X. The voltage at the load is given as,

$$V_L = \frac{\alpha_{SIN} \cdot V_{SIN}}{\alpha_X \cdot R_X} \cdot R_L \tag{8}$$

where R_L, is the load resistance measured accurately with an LCR meter. The voltage, V_L, is measured using an oscilloscope and includes the calibration coefficients α_{SIN} and α_X. Voltage at the output of the readout chain, V_O includes the calibration coefficients, α_G, α_{SIN} and α_X and is given as,

$$V_O = \frac{\alpha_{SIN} \cdot V_{SIN}}{\alpha_X \cdot R_X} \cdot \alpha_S \cdot R_S \cdot \alpha_G \cdot G \ , \tag{9}$$

where, α_S is the unknown calibration coefficient per channel to be determined, R_S is the sense resistor, α_G is the gain coefficient per channel determined by configuring all channels in voltage readout mode (Equation. 6), and G is the selected gain of the voltage readout channel. By measuring voltages V_L, and V_O, the effect of calibration coefficients α_{SIN} and α_X is accounted for. Using equation 8 and 9,

$$\alpha_S = \frac{V_O \cdot R_L}{V_L \cdot R_S \cdot \alpha_G \cdot G} \tag{10}$$

Calibration matrices are computed with channel # 1 as the reference. The calculations are shown for one channel configured as the current-source and the above procedure is repeated for all channels and desired frequencies at which the EIT system will operate. Details of the entire calibration procedure is illustrated in the flowchart of Fig. 25.

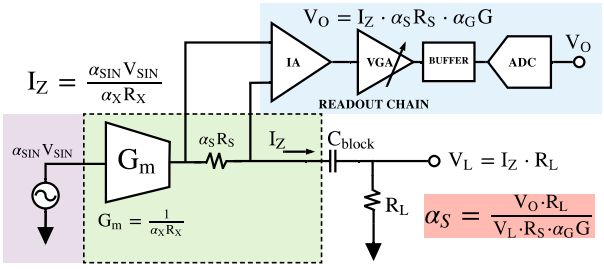

Fig. 24. Calibration circuit for a channel in the EIT system in the current-source mode. Variations due to AD9834 output, on-chip resistors and readout chain gain variation are analyzed. Calibration coefficient for each channel is calculated and normalized against a single channel.

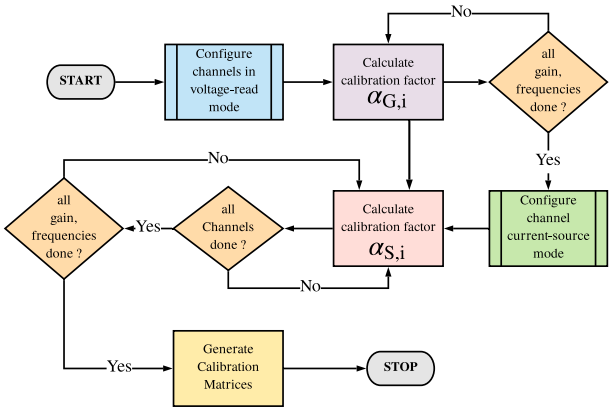

Fig. 25. Calibration procedure flowchart to calculate the calibration coefficients for the EIT system.

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