A Constant g_{m} Current Reference Generator with Purely Off-Chip Resistor

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***Abstract*—Most analog circuits need a current reference generator to provide a stable biasing point for the transistors. Given the limited voltage headroom in advanced node technologies, there would be notable restrictions on the tolerance of the reference current deviation. Use of off-chip reference generators adds to the size of the system while the on-chip reference current generators are still partially dependent on the on-chip resistor values which is prone to technology variations. We proposed an on-chip reference generator with a fully off-chip resistor which has less sensitivity to the process variations. Monte-Carlo simulation results shows that the proposed has 31% more precision compared to the conventional on-chip reference generator. Measurement results in 0.18 μm CMOS shows that the chip produces a stable reference current that is defined based on an off-chip resistor.**

***Index Terms*—Bias Generation, Reference Circuit, Constant Current Source, Constant g_{m}, Bandgap Reference**

I. Introduction

Constant transconductance (g_{m}) reference current generators are basic circuit building blocks, used to provide process-independent biases for operational amplifiers, voltage controlled oscillators, and sensor interfaces [1]–[3]. Generally, constant g_{m} reference current generators produce a transconductance that is inversely-proportional to some resistor value [4]. To produce a precise current reference, the resistance is typically implemented as a high-precision off-chip resistor, in series with a smaller on-chip resistor [5]. Unfortunately, process variation of the on-chip resistor might necessitate post-silicon trimming, which is costly and undesirable for mass production.

In this paper, we propose a new constant g_{m} reference current generator that does not require any carefully-controlled on-chip resistor. This obviates the need for expensive post-silicon trimming. Our novel design produces a constant transconductance that depends solely on an off-chip, high-precision resistor.

II. Conventional g_{m} Reference

Figure 1 (a) shows the conventional split resistor (split R) implementation of a constant g_{m} reference current generator. Both branches carry the same current and transistors $\mathrm{M}_{3,4}$ are of the same size while M_1 is M times larger than M_2. The voltage across the resistor R (the series combination of resistors r and R-r) is the difference between the gate-source voltages of M_2 and M_1 and will produce the bias current (I_{ref}). The bias current and the transconductance are calculated as

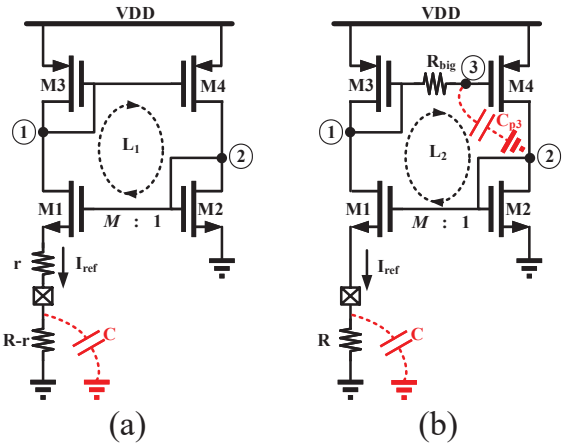

Fig. 1: Constant $\mathrm{g_m}$ reference current generators: (a) conventional, split R implementation (b) the proposed structure.

$$I_{\mathrm{ref}} = \frac{1}{R^2}\left(1-\frac{1}{\sqrt{M}}\right)^2 \frac{2}{\mu_{\mathrm{n}} C_{\mathrm{ox}} W/L} \tag{1}$$

$$g_{\mathrm{m1}} = \frac{2}{R}\left(1-\frac{1}{\sqrt{M}}\right) \tag{2}$$

where W, L, μ_n and C_{ox} are respectively the width, length, electron mobility, and oxide capacitance of M_2. As Eq. 2 shows, g_{m1} is dependent only on the resistance, R, and transistor sizing ratios. It would be robust to process variation, save for the on-chip r being part of the total resistance. But r is necessary to keep this circuit stable, as we show with the following analysis.

The loop L_1 in Fig. 1 (a) has one dominant zero and one dominant pole:

$$\omega_{\mathrm{z1}} = \frac{1}{(R-r)C} \quad , \quad \omega_{\mathrm{p1}} = \frac{1+g_{\mathrm{m1}}R}{1+g_{\mathrm{m1}}r}\cdot\omega_{\mathrm{z1}} \tag{3}$$

where C represents the parasitic off-chip capacitor. The loop gain ($A_{\mathrm{v}}(s)$) is calculated as

$$A_{\mathrm{v}}(s) = A_0\frac{(1-s/\omega_{\mathrm{z1}})}{(1-s/\omega_{\mathrm{p1}})} \quad , \quad A_0 = \frac{M}{3\sqrt{M}-2}. \tag{4}$$

The positive feedback of the loop is not a concern for $M < 4$ because the DC gain is lower than unity. However, at high frequencies, the loop gain is

$$A_{\rm v}(|s| >> \omega_{\rm p1}) = \frac{1+g_{\rm m1}R}{1+g_{\rm m1}r}.\frac{M}{3\sqrt{M}-2} \tag{5}$$

which is higher than unity if r = 0 (note that M = 2 and 3 are the only options), meaning that the loop is unstable without use of the on-chip portion. As depicted in Fig. 2 (a), this happens because $\omega_{\rm z1}$ has a lower frequency compared to $\omega_{\rm p1}$ and hence gives rise to the gain and pushes it beyond unity while the loop phase is close to zero. The loop has a positive gain so a loop phase equal to zero will cause instability. To ensure that the circuit is stable, we need a non-zero value of r, specifically

$$r > \frac{R}{2}\sqrt{M}. \tag{6}$$

This helps because the on-chip portion of the resistor gives us the leverage to move the pole to a lower frequency while the zero frequency remains the same. As shown in Fig. 2 (b) this can prevent the instability by keeping the high frequency loop gain below unity.

III. Proposed Constant $g_{\rm m}$ Reference Generator

The proposed structure shown in Fig. 1 (b) uses completely off-chip resistor and has the same transistor sizing as Fig. 1 (a). It has an additional pole due to $\rm R_{big}$ and the parasitic capacitor on node 3. Knowing that the poles at nodes 1 and 2 are at high frequencies due to the low resistance of these nodes, the loop gain is now calculated as

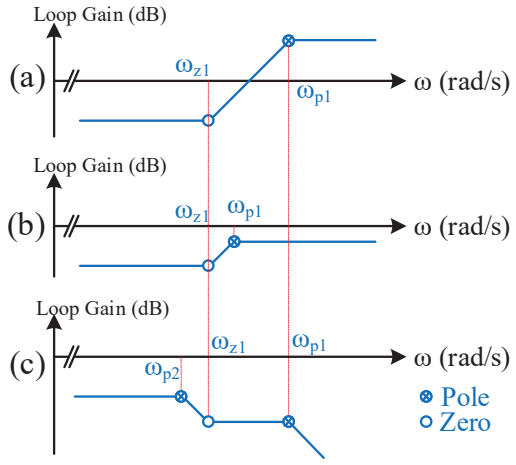

Fig. 2: Bode plot sketch of the loop gain: (a) non-compensated (b) conventional, split R implementation (c) the proposed structure.

$$A_{\rm v}(s) = A_0\frac{(1-s/\omega_{\rm z1})}{(1-s/\omega_{\rm p1})(1-s/\omega_{\rm p2})}\ ,\ A_0 = \frac{M}{3\sqrt{M}-2} \tag{7}$$

in which

$$\omega_{\rm z1} = \frac{1}{RC}\ ,\ \omega_{\rm p1} = (1+g_{\rm m1}R)\omega_{\rm z1}\ ,\ \omega_{\rm p2} = \frac{1}{R_{\rm big}C_{\rm p3}}. \tag{8}$$

The $C_{\rm p3}$ in Eq. 8 stands for the parasitic capacitor at node 3 and is mainly produced by gate-source capacitance of $\rm M_{4b}$. High values of $\rm R_{big}$ lead to $\omega_{\rm p2}$ smaller than $\omega_{\rm z1}$ and provides a stable system with the Bode plot shown in Fig. 2 (c). $\rm R_{big}$ can be implemented by use of one small size MOSFET and does not add considerable amount of area. The value of R in Eq. 1 and Eq. 2 now can be highly precise which leads to a more accurate $I_{\rm ref}$ and $g_{\rm m1}$.

IV. Implementation and Comparison

Figure 3 shows the implementation of the proposed design which is composed of four sections. The core bias circuit has the structure of Fig. 1 (b) with the addition of cascode transistors ($\rm M_{2a,b}$ and $\rm M_{3a,b}$) to decrease the channel length modulation on the mirroring transistors ($\rm M_{1a,b}$ and $\rm M_{4a,b}$). M is chosen to be 3 which means that $\rm M_{1a}$ is 3 times larger than $\rm M_{1b}$; this is achieved by choosing a multiplier of 3 for $\rm M_{1a}$ in order to obtain acceptable matching. R is chosen to be 5.7 kΩ which provides 40.6 μA reference current. The other section is the start-up circuit which will be addressed later.

Two sections in Fig. 3 implement Minch structure [6] for providing biasing voltages ($V_{\rm b2}$ and $V_{\rm b3}$) for the cascode transistors $\rm M_{2a,b}$ and $\rm M_{3a,b}$. At the $\rm V_{b2}$ bias generation, $\rm M_{7a,b}$ and $\rm M_{8a,b}$ mirror the current of the core bias circuit. $\rm M_{5a}$ has the same size as the $\rm M_{1b}$ while the $\rm M_{6a}$ is a big size device biased very close to sub-threshold. Consequently, the voltage at node A is equal to $V_{\rm eff,M1b}$ (= $V_{\rm GS,M5a}$ - $V_{\rm GS,M6a}$ $\approx$ $V_{\rm GS,M5a}$ - $V_{\rm th,M6a}$). $\rm M_{M6b}$ and $\rm M_{M2a,b}$ are of the same size and carry the same current, hence their $V_{\rm GS}$ is equal. The $\rm b_2$ node voltage could be calculated as

$$V_{\rm b2} = V_{\rm eff,M1b} + V_{\rm GS,M2b}. \tag{9}$$

Applying this voltage to the gate of $\rm M_{2a,b}$ provides enough voltage for $\rm M_{1a,b}$ to stay in saturation. The same situation happens in the Minch $\rm V_{b3}$ bias generation section by choosing $\rm M_{11b}$ as a big size near sub-threshold driven device which sets the node B voltage to $V_{\rm DD}$ - $V_{\rm eff,M4b}$.

The circuit has two states, one with $I_{\rm ref}$ equal to the value defined by equation 1 and the other with zero current. To make sure we do not end up with the latter, we use the start-up circuit that changes the state to the desired one and then turns off to have a minimal effect on the main circuit. Looking at the start-up section in Fig. 3, if node $\rm b_1$ voltage is zero (undesirable state), $\rm M_{s1}$ and $\rm M_{s2}$ act as an inverter that turns on $\rm M_{s3}$ and $\rm M_{s4}$; these then turn on $\rm M_{3a,b}$ and $\rm M_{4a,b}$ and flow current into the branches and increase the $\rm b_1$ and $\rm b_2$ node voltages to the the desirable state. The next step is to turn off the start-up circuit. $\rm M_{s2}$ is a small size device acting as a resistor; once

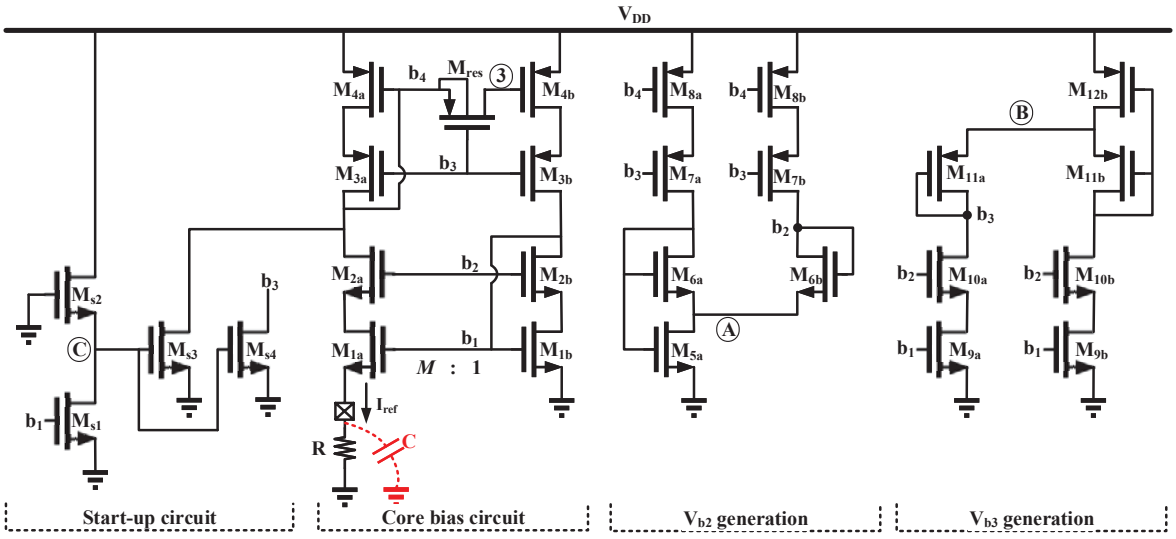

Fig. 3: The transistor-level implementation of the proposed structure

the circuit is back to its normal operation, b_1 node voltage goes high, M_{s1} turns on and sets the node C voltage to zero and turns off M_{s3} and M_{s4} to prevent them from affecting the circuit normal operation.

M_{res} (in Fig. 3) implements the R_{big} in Fig. 1 (b) and has a resistance of 2.7 MΩ; the parasitic capacitance at node 3 is equal to 842 fF which yields a pole frequency of 491 krad/s (78 kHz). This is lower than the zero frequency of 3.5 Mrad/s (557 kHz) considering an off-chip parasitic capacitor (C) of 50 pF. To have a fair comparison, a split structure has been implemented with all device sizing similar to Fig. 3. The only difference is removal of the M_{res} and addition of 30% of the resistance on-chip (r = 1.7 kΩ, R-r = 4 kΩ). These values will not satisfy Eq. 6 but the loop has a below unity value because of the body effect of M_{1a} which decreases the g_{m2}. The split also has been simulated with r = 0 to implement a non-compensated loop. Figure 4 shows the simulation results for the loop gain and phase considering 50 pF parasitic off-chip capacitor for all three cases. The gain for the non-compensated loop exceeds unity at frequencies higher than 300 kHz while it always stay below unity for the two other cases.

In order to characterize the mismatch and process variations sensitivity, Monte-Carlo simulations has been performed on the conventional split R and the proposed design. Figure 5 (a) and 5 (b) show the results for 200 iterations. The proposed structure has lower dispersion compared to the split R which leads to 31% reduction in the standard deviation. This improvement is the result of removing the on-chip part of the resistor which results in higher precision. The deviation in the proposed design is caused by the mismatch between transistors as well as the process variations on the MOSFET process transconductance (depicted on Eq. 1 and Eq. 2).

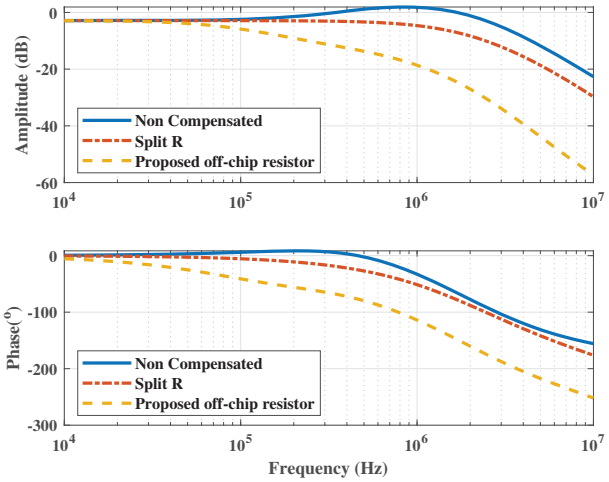

Fig. 4: Bode plot of the amplitude and phase of the loop gain for all three structures.

V. Measurement Results

Both the split R and the proposed structure were fabricated on the same chip in a 0.18 μm CMOS technology, each occupying an area of 0.13×0.24 mm^2. Figure 6 (a) shows the layout implementation of the proposed structure. The layout for the conventional, split R structure has the same size with little differences.

The die micrograph is shown in Fig. 6 (b). The target reference current is 40.6 μA and measurement results of the sample chip show 42.1 μA for the split-R structure and 51.2 μA for the proposed structure. The source of this discrepancy is the physical distance between the proposed circuit and ground. Figure 6 (b) shows the distance between the proposed

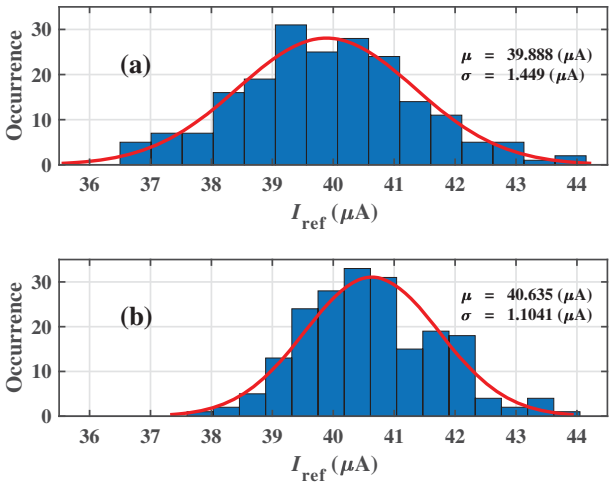

Fig. 5: Monte-Carlo simulation results: (a) split R implementation (b) the proposed structure.

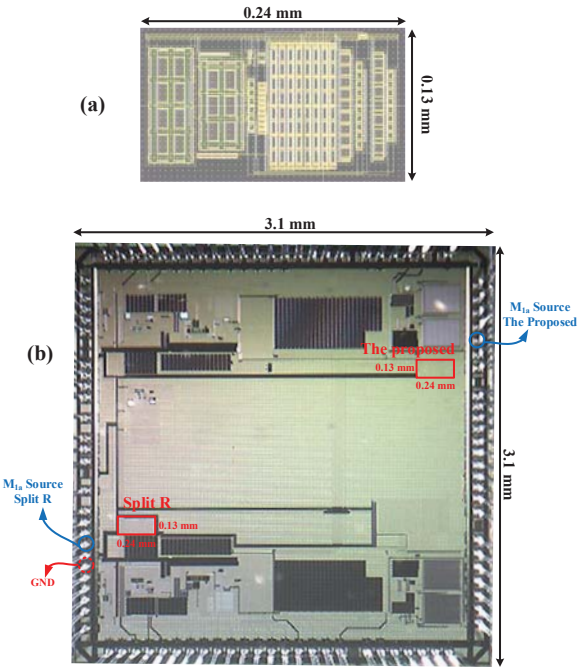

Fig. 6: The implementation (a) layout of the proposed reference current generator in 0.18 μm technology (b) the die micrograph of the fabricated chip.

circuit and ground is considerably higher than for the conventional one. Hence, the trace connecting proposed design to the ground produces a non-zero voltage due to its resistive voltage drop. In other words, the voltage of the ground connected to the bottom of R (Fig. 3) is still zero (because of the short distance) while all other grounds are connected to a biased ground with the voltage of some few millivolts. The voltage across R is now calculated as

$$V_{\mathrm{R}} = V_{\mathrm{GND,1b}} + V_{\mathrm{GS,1b}} - V_{\mathrm{GS,1a}} - V_{\mathrm{GND,R}} \qquad (10)$$

in which $V_{\mathrm{GND,1b}}$ defines the voltage of the ground connected to the source of $\mathrm{M_{1b}}$ and $V_{\mathrm{GND,R}}$ defines the voltage of the ground connected to the bottom of R. Consequently, the voltage across R is approximated to

$$V_{\mathrm{R}} = V_{\mathrm{GS,1b}} - V_{\mathrm{GS,1a}} + V_{\mathrm{GND,1b}}. \qquad (11)$$

This V_{R} is higher than the designated voltage and increases the reference current produced by the proposed circuit. The conventional design is placed close to the chip ground and does not suffer this problem as much as the proposed does. This can be solved in a careful design which places the bias current generator block close to the chip ground or specifies a separate ground for it.

VI. Conclusion

A new proposed structure for implementing a constant g_{m} reference bias generator is presented that does minimum changes on the conventional circuit, keeps the structure stable and alleviates the sensitivity to the on-chip resistor deviations. This decreases the reference current deviations by 31% according to the simulation results. Implementation shows that the proposed structure is stable and provides a constant current.

VII. Future Work

Off-chip resistors with different temperature coefficients can provide a temperature-independent current or transconductance. Also, the proposed can be used for bandgap voltage or current references that are intended to be proportional to absolute temperature (PTAT) or complementary to absolute temperature (CTAT) or temperature independent by use of purely off-chip resistors with any desired thermal coefficient.

VIII. Acknowledgments

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References

[1] J. M. Steininger, "Understanding wide-band mos transistors," *IEEE Circuits and Devices Magazine*, vol. 6, no. 3, pp. 26–31, 1990.

[2] S. Nicolson and K. Phang, "Improvements in biasing and compensation of cmos opamps," *Analog Integrated Circuits and Signal Processing*, vol. 43, no. 3, pp. 237–245, 2005.

[3] T. Delbrück and A. Van Schaik, "Bias current generators with wide dynamic range," *Analog Integrated Circuits and Signal Processing*, vol. 43, no. 3, pp. 247–268, 2005.

[4] D. A. Johns and K. Martin, *Analog integrated circuit design*. John Wiley & Sons, 2008.

[5] W. K.-w. Tong, *A GHz CMOS frequency synthesizer for mobile communication*. University of Toronto, 1999.

[6] B. A. Minch, "A low-voltage mos cascode bias circuit for all current levels," in *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No. 02CH37353)*, vol. 3. IEEE, 2002, pp. III–III.