A Constant g_m Current Reference Generator With Pseudo Resistor-Based Compensation

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***Abstract*— Most analog circuits need a current reference generator to provide a stable biasing point for the transistors. Given the limited voltage headroom in advanced node technologies, there would be notable restrictions on the tolerance of the reference current deviation. Use of off-chip reference generators adds to the size of the system while the on-chip reference current generators are still partially dependent on the on-chip resistor values which is prone to technology variations. We propose an on-chip reference generator with a fully off-chip resistor which has less sensitivity to process variations. Monte-Carlo simulation results shows that the proposed has 31% more precision compared to the conventional on-chip reference generator. Measurement results in 0.18 μm CMOS shows that the chip produces a stable reference current that is defined based on an off-chip resistor. The proposed structure consumes the same current as conventional and does not add to the power consumption.**

***Index Terms*— Bias generation, reference circuit, constant current source, constant g_m, bandgap reference.**

I. Introduction

THE constant transconductance (g_m) current reference is a small but critical component in analog integrated circuits. It provides reliable, process-independent biasing for a wide range of common circuit blocks, from operational amplifiers and voltage controlled oscillators to signal converters [1]–[3].

The g_m reference current generator produces a transconductance that is inversely proportional to a known resistance value [4]. And to ensure a highly accurate transconductance, this resistance is typically implemented as a high-precision off-chip resistor. Unfortunately, the off-chip resistor, together with the parasitic capacitance at its bonding pad connection, forms a dominant pole-zero doublet that makes the g_m reference circuit an unstable system [2].

One common approach to stabilizing the g_m reference circuit is to compensate it with a large, drawn capacitor that is on the same order of magnitude as the bonding pad's parasitic capacitance. The cost of this strategy is that the compensation capacitor would require either a significant amount of chip area (if implemented on chip), or the use of an extra bonding pad and an extra component (if implemented off-chip) [3]. Some modifications have been proposed to reduce the size of the compensation capacitor [2], but these necessitate extra circuitry that degrades the g_m reference circuit's robustness to device mismatch [5].

Another popular method for compensating the g_m circuit is to implement a portion of its resistor on the chip [6]. In this case, the transconductance is inversely proportional to the series combination of the on-chip and off-chip resistors, but the circuit's dominant pole is now at a low enough frequency that the circuit is no longer unstable. The disadvantage of using a portion of the resistor on-chip is that it makes the g_m reference generator susceptible to resistor variation; this is typically addressed with post-silicon trimming, which is costly and undesirable for mass production.

To address these shortcomings, we recently proposed a new constant g_m reference current generator that depends solely on an off-chip, high-precision resistor [7]. It is inherently stable, without the need for a compensation capacitor, an on-chip resistor, or extra circuitry that would diminish its robustness to process variation and device mismatch. In this paper, we analyze our g_m reference current generator's sensitivity to process variations as well as device mismatch in comparison to that of a conventional architecture. Also, we present a complete, formalized design methodology for our proposed g_m reference circuit. Finally, we identify and address practical implementation concerns. For completeness, we also include our previously-presented experimental results from [7].

II. Conventional g_M Reference

Figure 1a shows the split resistor (split R) implementation of a constant g_m reference current generator, which uses an on-chip resistor to stabilize the loop. Both branches in Fig. 1a carry the same amount of current and transistors $M_{3,4}$ are of the same size, while M_1 is M times larger than M_2. The voltage across the resistor R (the series combination of resistors r and R-r) is the difference between the gate-source voltages of M_2 and M_1 and will produce the bias current (I_{ref}). The bias current and the transconductance are calculated as

$$I_{\text{ref}} = \frac{1}{R^2}\left(1-\frac{1}{\sqrt{M}}\right)^2 \frac{2}{\mu_n C_{\text{ox}} W/L}, \tag{1}$$

$$g_{m1} = \frac{2}{R}\left(1-\frac{1}{\sqrt{M}}\right), \tag{2}$$

where W, L, μ_n and C_{ox} are respectively the width, length, electron mobility, and oxide capacitance of M_2. As Eqn. 2

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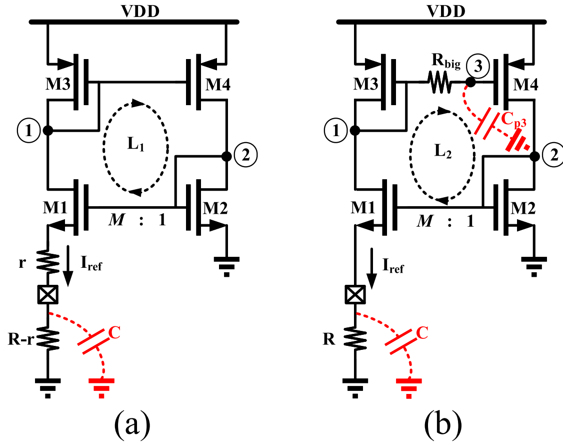

Fig. 1. Constant g_m reference current generators: (a) conventional, split R implementation (b) the proposed structure.

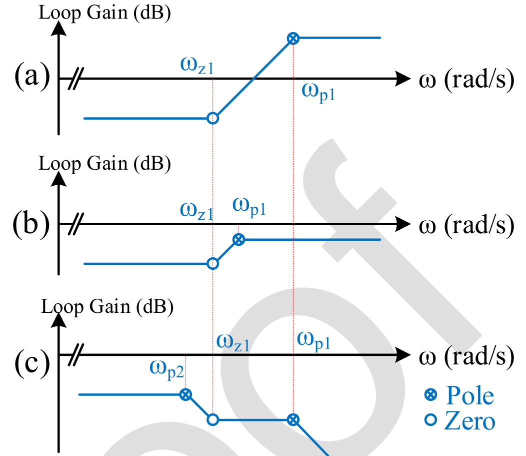

Fig. 2. Bode plot sketch of the loop gain: (a) non-compensated (b) conventional, split R implementation (c) the proposed structure.

shows, g_{m1} is dependent only on the resistance, R, and transistor sizing ratios. It would be robust to process variation, save for the on-chip r being part of the total resistance. But r is necessary to keep this circuit stable, as we show with the following analysis.

The loop L_1 in Fig. 1a has one dominant zero and one dominant pole (see derivation in Section A of Appendix):

$$\omega_{z1} = \frac{1}{(R-r)C} \quad , \quad \omega_{p1} = \frac{1+g_{m1}R}{1+g_{m1}r} \cdot \omega_{z1}, \tag{3}$$

where C is the parasitic off-chip capacitor. The loop gain ($A_v(s)$) is calculated as

$$A_v(s) = A_0 \frac{(1-s/\omega_{z1})}{(1-s/\omega_{p1})} \quad , \quad A_0 = \frac{M}{3\sqrt{M}-2}. \tag{4}$$

As shown in Eqn. 53 in Section A of the Appendix, the loop gain at high frequencies is

$$A_v(|s| \gg \omega_{p1}) = \frac{\sqrt{M}}{1+g_{m1}r} \tag{5}$$

If $r = 0$, then Eqn. 5 can be simplified to

$$A_v(|s| \gg \omega_{p1}) = \sqrt{M}, \tag{6}$$

which is higher than unity because M is always higher than unity. As illustrated in Fig. 2a, this happens because ω_{z1} causes the gain to increase beyond unity while the loop phase is close to zero. The loop has a positive gain so a loop phase equal to zero will cause instability, this happens at high frequencies where the pole and zero cancel each other's phases and the loop phase will become zero. To ensure that the circuit is stable, we need a non-zero value of r, specifically

$$r > \frac{R}{2}\sqrt{M}. \tag{7}$$

This helps because the on-chip portion of the resistor gives us the leverage to move the pole to a lower frequency while the zero frequency remains the same. As shown in Fig. 2b, this can prevent instability by keeping the high frequency loop gain below unity. The cost of this approach is that the resulting transconductance is susceptible to variations in the value of r.

III. Proposed g_m Reference

Figure 1b shows a simplified schematic of our proposed g_m current reference generator. The transistor sizing is the same as in Fig. 1a, and the resistor R is implemented completely off-chip. This means that the value of R in Eqn. 1 and Eqn. 2 can be tightly controlled with precision components, which leads to a more accurate I_{ref} and g_{m1}. Our proposed structure includes a new component, R_{big}. This is a large resistor which, together with the parasitic capacitance on the gate of transistor M_4, creates a dominant pole that starts decreasing the gain at low frequencies and stabilizes the circuit. While R_{big} must be large enough (see Section III-B) for this scheme to work, it does not have to be precisely controlled, and the reference current or transconductance value that the g_m circuit produces is independent of the absolute value of R_{big}.

A. Loop Gain Analysis

With the introduction of a new pole, ω_{p2}, due to R_{big}, the loop gain of our proposed structure can be written as

$$A_v(s) = A_0 \frac{(1-s/\omega_{z1})}{(1-s/\omega_{p1})(1-s/\omega_{p2})}, \quad A_0 = \frac{M}{3\sqrt{M}-2}, \tag{8}$$

where

$$\omega_{z1} = \frac{1}{RC} \ , \ \omega_{p1} = (1+g_{m1}R)\omega_{z1} \ , \ \omega_{p2} = \frac{1}{R_{big}C_{p3}}. \tag{9}$$

The C_{p3} in Eqn. 9 stands for the parasitic capacitor at node 3 and is mainly produced by the gate-source capacitance of M_4. High values of R_{big} lead to ω_{p2} smaller than ω_{z1} and provide a stable system with the Bode plot shown in Fig. 2c. R_{big} can be implemented with a transistor that does not add considerable amount of area. The R_{big} resistor does not consume any DC current, and, as we discuss in the following section, it is biased with circuitry that is already present in the conventional g_m reference circuit. As such, our proposed structure does not cost any extra power consumption.

B. Implementing R_{big}

As we saw from the loop gain analysis, we can ensure that our circuit remains stable provided the ω_{p2} pole occurs at a

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lower frequency than the ω_{z1} zero. Designing ω_{p2} close to ω_{z1} would jeopardise the circuit's stability, because imperfections in the fabrication process could swap their relative locations (i.e. place $\omega_{z1} < \omega_{p2}$). Pushing the ω_{p2} to lower frequencies guarantees a high safety margin the stability, but it slows down the start-up behavior. Given this trade-off between stability and speed, we found empirically that a reasonable margin of safety requires

$$\omega_{z1}/\omega_{p2} \gtrsim 5. \tag{10}$$

Since C_{p3} is a parasitic capacitance that depends on the size of M_4, the resistance R_{big} is the only free design parameter that affects the ratio of ω_{z1} to ω_{p2}. With typical values of R_{big} falling in the MΩ range, this resistor would consume a lot of area if it were implemented on chip as a poly-resist component. A more area-efficient solution is to implement R_{big} as a triode-region transistor.

Figure 3a illustrates this idea, with the triode-region transistor M_{res} providing a pseudo-resistor implementation of R_{big}. The challenge of this approach lies in how to generate an appropriate bias voltage, denoted by the V_{bat} battery between the source and gate of M_{res}. If the M_{res} source-gate voltage is too small, it will be pushed into the subthreshold region, which would result in a resistor in the GΩ range [8]. This is not suitable for our application, because it will produce a ω_{p2} pole that has a very low frequency that slows down the start-up process.

To ensure that M_{res} operates just above the subthreshold region, we can bias its gate with a modified version of the low voltage cascode bias circuit that was first introduced by Minch [9]; the simplified version is shown in Fig. 3b and will be studied in more detail in section VI. With this cascode biasing circuit, the source-gate voltage of M_{res} is

$$V_{SG,Mres} = V_{b4} - V_{b3}, \tag{11}$$

where V_{b4} is the voltage produced by the diode connected transistor M_3 and can be calculated as

$$V_{b4} = V_{DD} - V_{SG,M3}. \tag{12}$$

Also, V_{b3} is given by

$$\begin{aligned} V_{b3} &= V_{DD} - V_{eff,M9} - V_{SG,M7} \\ &= V_{DD} - V_{eff,M9} - V_{SG,M3}, \end{aligned} \tag{13}$$

where we have used the fact that transistors M_4 and M_7 have the same size and the same amount of drain source current.

Substituting Eqns. 12 and 13 into Eqn. 11, the source gate voltage of M_{res} is

$$V_{SG,Mres} = V_{eff,M9} \tag{14}$$

Now, transistor M_9 is the same size as M_3, but it carries twice the drain source current. This implies $V_{eff,M9} = \sqrt{2}V_{eff,M3} = \sqrt{2}V_{eff}$. So, the effective voltage of M_{res} can be written as

$$V_{eff,Mres} = \sqrt{2}V_{eff} - V_{th} \tag{15}$$

Let us assume that the technology has the necessary voltage headroom to keep $V_{SG,Mres}$ higher than the threshold voltage

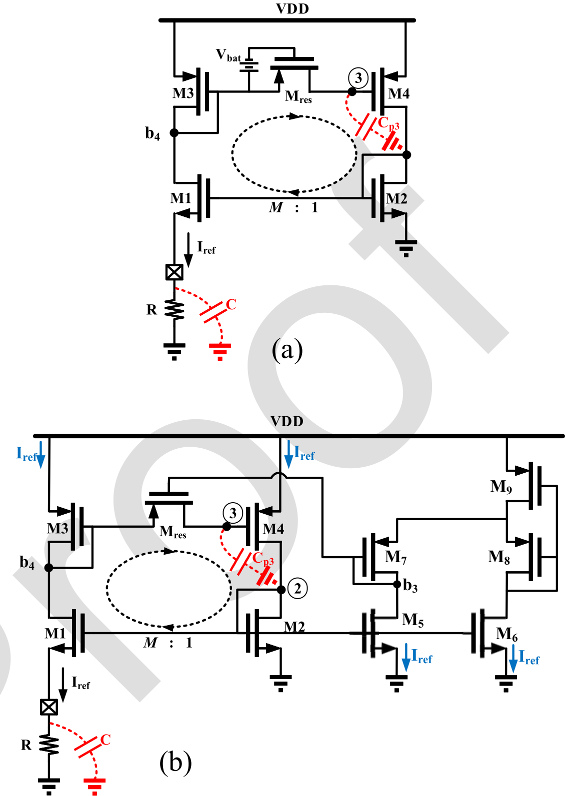

Fig. 3. The proposed implementation of R_{big}: (a) hypothetical implementation using a battery (b) practical implementation using a bias voltage.

so that we can avoid the sub-threshold region. This is particularly important because sub-threshold might lead to a very high resistor value which might not be desirable. The current versus voltage formula for the triode region is

$$I_{DS} = \mu_p C_{ox} \frac{W}{L} V_{eff,Mres} V_{DS} \tag{16}$$

so the resistance R_{big} is calculated as

$$R_{big} = \frac{1}{\mu_p C_{ox} \frac{W}{L}(\sqrt{2}V_{eff} - V_{th})}. \tag{17}$$

The parasitic capacitor at node 3 is mostly produced by the gate-source of M_4 which can be calculated as

$$C_{p3} = 2/3 W_{M4} L_{M4} C_{ox}. \tag{18}$$

So, the ω_{p2} can be calculated as

$$\omega_{p2} = \mu_p \frac{W_{Mres}}{L_{Mres}} \frac{3}{2 W_{M4} L_{M4}} (\sqrt{2}V_{eff} - V_{th}). \tag{19}$$

Now, we can calculate the size of M_{res} based on Eqn. 10:

$$\frac{W_{Mres}}{L_{Mres}} < \frac{2 W_{M4} L_{M4}}{15 RC \mu_p (\sqrt{2}V_{eff} - V_{th})}. \tag{20}$$

To avoid instability due to temperature variation, the W/L ratio of M_{res} must be chosen well within this allowable range.

IV. Design Methodology for Proposed g_M Reference

To design our proposed g_m reference circuit (Fig. 3b) for a given current and/or transconductance value, the first step

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is to determine the W/L ratio of the primary transistor (that is, transistor M_2). This is typically derived from voltage headroom constraints. And from the W/L ratio, we can calculate the size of R and a convenient value for the ratio M (to size transistor M_1) via Eqn. 1. These first few steps in the design procedure are common to our architecture and to the more conventional g_m reference architectures [2], [3], [6], [10].

Transistors $M_{3,4}$ should be sized so that their effective voltage is larger than $V_{th}/\sqrt{2}$. Specifically, we choose

$$\frac{W_{M3}}{L_{M3}} < \frac{4I_{ref}}{V_{th}^2 \mu_p C_{ox}}. \tag{21}$$

This ensures that the modified Minch structure (transistors M_6 to M_9 of Fig. 3b) biases M_{res} to operate in the above threshold region.

The transistors in the modified Minch structure are sized based on the main g_m reference circuit: transistors $M_{5,6}$ are the same size as transistor M_2; transistors $M_{7,9}$ are the same size as $M_{3,4}$. Also, following [9], transistor M_8 is sized much larger than $M_{3,4}$.

Finally, we size M_{res} to meet the Eqn. 20 constraint, repeated here for clarity:

$$\frac{W_{Mres}}{L_{Mres}} < \frac{2W_{M4}.L_{M4}}{15RC\mu_p(\sqrt{2}V_{eff} - V_{th})}. \tag{22}$$

V. Sensitivity Analysis

The reference current is a function of process variations and mismatch. Process variations refers to the deviations that happens for all devices on the chip and the mismatch refers to the differences between the devices. Our analysis below shows that the reference current deviations are dominantly imposed by process variations and mismatch effect is negligible. We also do a comparison and show that the proposed is 50% less sensitive than the Split R structure in design technology.

A. Process Variations

Looking at Eqn. 1, the output current is a function of resistor, β ($= 1/2\mu_n C_{ox}$ W/L), and M. Because M is a ratio and not an absolute value, it is just showing up in our mismatch calculations. Considering process variation, the proposed structure is only affected by β:

$$\sigma^2_{\frac{\Delta I_{ref}}{I_{ref}}} = \sigma^2_{\frac{\Delta I_{ref}}{I_{ref}}}\Big|_{\beta,\text{process}} \tag{23}$$

while the conventional structure suffers from both β and on-chip resistor variation:

$$\sigma^2_{\frac{\Delta I_{ref}}{I_{ref}}} = \sigma^2_{\frac{\Delta I_{ref}}{I_{ref}}}\Big|_{\beta,\text{process}} + \sigma^2_{\frac{\Delta I_{ref}}{I_{ref}}}\Big|_{\text{r,process}} \tag{24}$$

In the 0.18 μm CMOS technology we used, β for a large square device has a standard deviation of

$$A_{\beta,\text{process}} = 0.444\mu m. \tag{25}$$

TABLE I

Simulation Condition for Sensitivity Analysis of Fig. 1a,b Circuits

Device Name	Device Size
M1	$6 \times (1 \times 7.5\mu m)/15\mu m$
M2	$2 \times (1 \times 7.5\mu m)/15\mu m$
M3	$8 \times (1 \times 2.5\mu m)/10\mu m$
M4	$8 \times (1 \times 2.5\mu m)/10\mu m$
R	5742Ω
r	2871Ω

According to Eqn. 57 in Section B of Appendix, the reference current deviation because of this is calculated as

$$\sigma^2_{\frac{\Delta I_{ref}}{I_{ref}}}\Big|_{\beta,\text{process}} = \frac{A^2_{\beta,\text{process}}}{W \times L} \tag{26}$$

For a 15 μm/15 μm device, the normalized standard deviation is calculated as 0.0296.

As calculated in Eqn. 62 in Section B of Appendix, deviations in the on-chip portion of the resistor can be calculated as

$$\sigma^2_{\frac{\Delta I_{ref}}{I_{ref}}}\Big|_{\text{r,process}} = \left(\frac{A_{\text{r,process}}}{W}\right)^2 \cdot \left(2\frac{r}{R}\right)^2 \tag{27}$$

in which $A_{\text{r,process}}$ refers to the process variations modeled as the physical deviation in the width of the resistors (ΔW); in our technology its value is

$$A_{\text{r,process}} = 0.06\mu m. \tag{28}$$

For the split R structure, assuming the least on-chip portion of 50% (Eqn. 7), the normalized standard deviation based on Eqn. 27 is calculated as 0.030. In practice, some safety margin seems necessary so the on-chip portion should be higher than 50% which leads to even higher deviations.

To match the calculation and the simulation results, the two circuits presented in Fig. 1a,b were designed with the table I device sizes.

We performed Monte-Carlo simulations and just included the process variations. The normalized standard deviation of the current produced by figure 1b is 0.022 which is close to the 0.0296 calculated above. Note that this structure uses a high precision off-chip resistor and hence the β variations are the only factor. The normalized standard deviation caused by the process variations in the resistor is 0.027 which is also close to the 0.03 calculated above.

B. Mismatch

Section C of appendix uses Pelgrom law [5] and calculates the current deviation caused by mismatch in the NMOSs (M_1 and M_2):

$$\sigma^2_{\frac{\Delta I_{ref}}{I_{ref}}}\Big|_{\text{NMOS}} = \frac{A^2_{\beta,n}}{W \times L} \cdot \frac{M + 1/M}{\left(\sqrt{M} - 1\right)^2} + \frac{A^2_{Vth,n}}{W \times L} \cdot \frac{(M^2 + M)(\beta R)^2}{\left(\sqrt{M} - 1\right)^4}. \tag{29}$$

TABLE II
PELGROM COEFFICIENTS OF THE USED 0.18 μM CMOS TECHNOLOGY

Parameter	Value
$A_{\beta,n}$	0.0098 μm
$A_{Vth,n}$	9.24 $\times 10^{-3} V \mu m$
$A_{\beta,p}$	0.0094 μm
$A_{Vth,p}$	5.47 $\times 10^{-3} V \mu m$
β_n	95 $\times 10^{-6} V^2/A$

The mismatch produced by the PMOS is calculated as

$$\sigma^2_{\frac{\Delta I_{\rm ref}}{I_{\rm ref}}}\bigg|_{\rm PMOS} = A^2_{\beta,\rm p}\frac{1}{W \times L} + A^2_{\rm Vth,p}\frac{2/V_{\rm eff}}{W \times L} \quad (30)$$

The Pelgrom coefficients of our technology are listed in table II. The effective voltage of the PMOS is 1.128 V based on simulations, so the overall standard deviation of current based on mismatch is calculated as:

$$\sigma^2_{\frac{\Delta I_{\rm ref}}{I_{\rm ref}}}\bigg|_{\rm mismatch} = 0.004 \quad (31)$$

which is close to 0.0034 produced by the simulation results. This is 7 times lower than the process variations of the proposed structure so the process variations has a dominant effect.

VI. FULL IMPLEMENTATION OF PROPOSED $g_{\rm m}$ REFERENCE

A. Cascode Implementation

Figure 4 shows the cascode implementation of the proposed design which is composed of four sections. The core bias circuit has the structure of Fig. 1b with the addition of cascode transistors (M_{1b}, M_{2b}, M_{3b}, and M_{4b}) to decrease the channel length modulation on the mirroring transistors (M_{1a}, M_{2a}, M_{3a}, and M_{4a}).

Two sections in Fig. 4 implement Minch structure [9] for providing biasing voltages (V_{b2} and V_{b3}) for the cascode transistors M_{1b} and M_{2b} as well as M_{3b} and M_{4b}. At the V_{b2} bias generation, $M_{13a,b}$ and $M_{14a,b}$ mirror the current of the core bias circuit. Let us say we size all transistors in the main branches of the circuit ($M_{1a,b}$, $M_{2a,b}$, $M_{3a,b}$, and $M_{4a,b}$) so that they have the same effective voltage. M_{10} has the same size as the M_{2a} but is carrying 2X current (currents mirrored by M_{13a} and M_{14a} passes through it). We define the effective voltage as the difference of the gate-source voltage and the threshold voltage, we will have

$$V_{\rm eff,M10} \simeq \sqrt{2}V_{\rm eff,M2a} = \sqrt{2}V_{\rm eff,NMOS}. \quad (32)$$

The voltage at node A is the difference between gate-source voltages of M_{10} and M_{11}:

$$V_A = V_{\rm GS,M10} - V_{\rm GS,M11} \quad (33)$$

The transistors have the same threshold voltage so

$$V_A = V_{\rm eff,M10} - V_{\rm eff,M11}. \quad (34)$$

M_{11} is N times larger than M_{10} while carrying half of the current, so its effective voltage is:

$$V_{\rm eff,M11} = \frac{V_{\rm eff,M10}}{\sqrt{2N}}. \quad (35)$$

If N is high enough, the $V_{\rm eff,M11}$ is negligible compared to that of $V_{\rm eff,M10}$, so we can approximate Eqn.34 to

$$V_A \simeq V_{\rm eff,M10}. \quad (36)$$

Substituting Eqn.32 into Eqn. 36 we have

$$V_A \simeq \sqrt{2}V_{\rm eff,NMOS}. \quad (37)$$

M_{12}, M_{1b}, and M_{2b} are of the same size and carry the same amount of current, hence have identical gate-source voltages. The b_2 node voltage could be calculated as

$$V_{\rm b2} = \sqrt{2}V_{\rm eff,NMOS} + V_{\rm GS,M2b}. \quad (38)$$

Applying this voltage to the gate of M_{1b} and M_{2b} provides $\sqrt{2}V_{\rm eff,NMOS}$ drain-source voltage for M_{2a} to stay in saturation.

Note that in original Minch structure, the current passing through $M_{13a,b}$ is negligible compared to $M_{14a,b}$ current, so the current passing through M_{10} is almost equal to that of M_{2a}. Consequently, the drain-source voltage provided for M_{2a} is exactly equal to $V_{\rm eff}$. We make $M_{13a,b}$ and $M_{14a,b}$ currents equal to be able to get a higher drain-source voltage for M_{2a}, this will further decrease the channel length modulation and help us get better matching results. For a more limited voltage headroom, the original Minch structure is recommended.

The same situation happens in the Minch V_{b3} bias generation section by choosing M_8 as a big size near sub-threshold driven device which sets the node B voltage to

$$V_{\rm B} = V_{\rm DD} - \sqrt{2}V_{\rm eff,PMOS} \quad (39)$$

which leads to

$$V_{\rm b3} = V_{\rm DD} - (\sqrt{2}V_{\rm eff,PMOS} + V_{\rm SG,M4b}). \quad (40)$$

B. Startup Circuit

The circuit has two states, one with $I_{\rm ref}$ equal to the value defined by Eqn. 1 and the other with zero current. To make sure we do not end up with the latter, we use the start-up circuit that changes the state to the desired one and then turns off to have a minimal effect on the main circuit. Looking at the start-up section in Fig. 4, if node b_1 voltage is zero (undesirable state), M_{s2} acts as a resistive load for M_{s1} so that they make an inverter with a '0' input that turns on M_{s3} and M_{s4}; these then turn on $M_{3a,b}$ and $M_{4a,b}$ and flow current into the branches and increase the b_1 and b_2 node voltages to the desirable state.

The next step is to turn off the start-up circuit. M_{s2} is a small size device acting as a resistor; once the circuit is back to its normal operation, b_1 node voltage goes high, M_{s1} turns on and sets the node D voltage to zero and turns off M_{s3} and M_{s4} to prevent them from affecting the circuit normal operation.

VII. DESIGN EXAMPLE

A sample circuit is implemented in 0.18 μm CMOS technology. Because of technology limitations, we had to modify the implementations in two ways:

(1) Limited voltage headroom does not allow us to have the exact $R_{\rm big}$ implementation provided above. We had to increase

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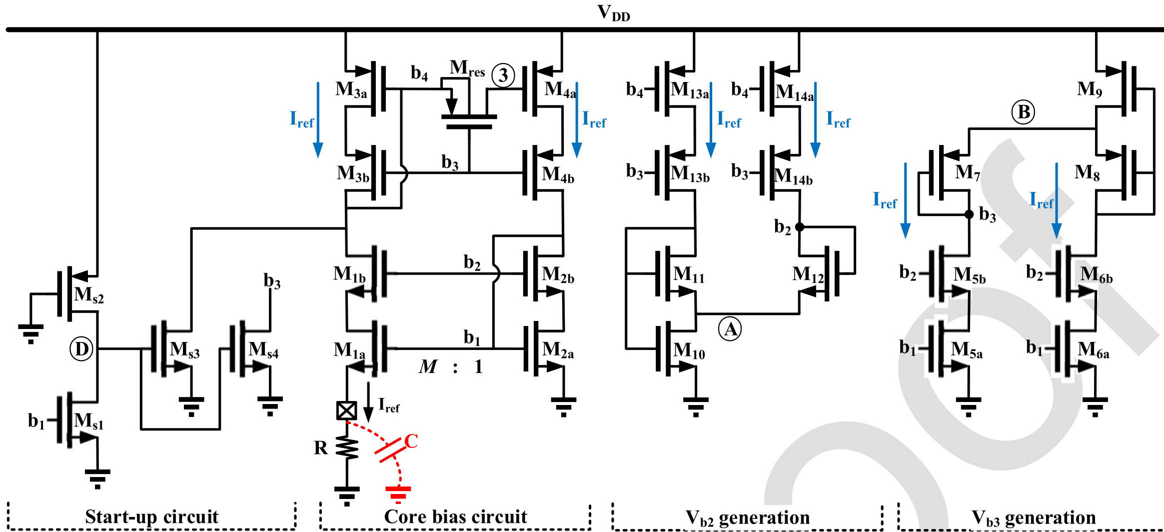

Fig. 4. The transistor-level implementation of the proposed structure.

the size of cascode devices (M_{1b}, M_{2b}, M_{3b}, and M_{4b}) so that they are closer to subthreshold region. This gives us the chance to keep M_{res} in active region and provide drain-source voltage for M_{1a}, M_{2a}, M_{3a}, and M_{4a}.

(2) We had to connect the body of transistor M_{1a} to the ground so there is a mismatch between the threshold voltage of M_{1a} and M_{2a}. This adds to the deviation but works in favor of the conventional structure because it decreases the effective transconductance of M_{1a} (g_{m1a} - $g_{m1a,b}$ with $g_{m1a,b}$ as the body effect transconductance) and helps us keep majority of resistor off-chip.

M is chosen to be 3 which means that M_{1a} is 3 times larger than M_{2a}; this is achieved by choosing a multiplier of 3 for M_{1a} in order to obtain acceptable matching. R is chosen to be 5.7 kΩ which provides 40.6 μA reference current.

M_{res} (in Fig. 4) implements the R_{big} in Fig. 1b and has a resistance of 2.7 MΩ; the parasitic capacitance at node 3 is equal to 842 fF which yields a pole frequency of 491 krad/s (78 kHz). This is lower than the zero frequency of 3.5 Mrad/s (557 kHz) considering an off-chip parasitic capacitor C of 50 pF. To have a fair comparison, a split structure has been implemented with all device sizing similar to Fig. 4. The only difference is removal of the M_{res} and addition of 30% of the resistance on-chip (r = 1.7 kΩ, R-r = 4 kΩ). These values will not satisfy Eqn. 7 but the loop gain has a below unity value because of the body effect of M_{1a} which decreases the g_{m1a}. The split also has been simulated with $r = 0$ to implement a non-compensated loop. Figure 5 shows the simulation results for the loop gain and phase considering 50 pF parasitic off-chip capacitor for all three cases. The gain for the non-compensated loop exceeds unity at frequencies higher than 300 kHz while it always stay below unity for the two other cases.

According to Eqn. 9, ω_{z1} is a function of R and C. R is the off-chip resistor and its value should be highly fixed so its variations will not be considerable. C is the total parasitic caps connected to the source of M_1 in Fig. 1; the two main contributors are the electrostatic discharge (ESD) protection and the parasitics from the board. Typical ESD caps for

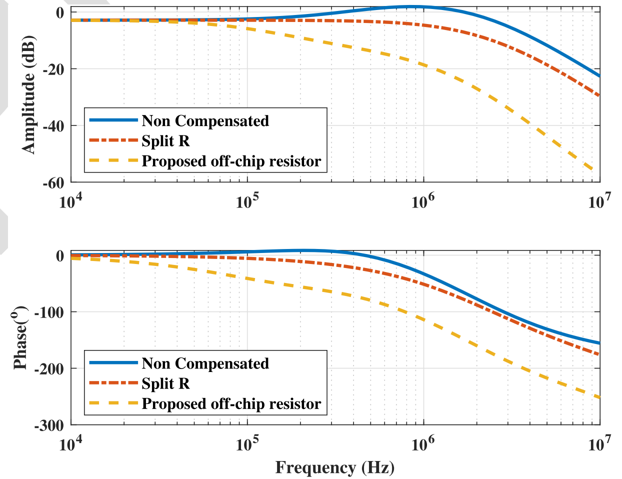

Fig. 5. Bode plot of the amplitude and phase of the loop gain for all three structures. The g_m reference circuit has a positive feedback, so a phase of zero with a gain higher than unity can lead to instability. From the Bode plot of the uncompensated structure, we observe that there will be oscillation at around 400 kHz, since the gain at this frequency is higher than one and phase is almost zero. The split R and our novel structure both keep the gain below unity, and so are stable.

0.18 μm CMOS are around 4 pF for an analog pin. The parasitic cap for a 3 cm long trace with a width of 1 mm is 3.6 pF in a typical PCB technology that uses FR4 board material [11]. It can be said that the value of C is lower than 8 pF. Use of a ceramic resistor for R does not add much to the parasitic cap but we foresaw use of potentiometers because this design is the initial prototype. We chose AD5121, a digital potentiometer produced by Analog Devices. The parasitic capacitance on the terminal for this particular device is 25 pF and we included this in our design. So, worst case parasitic capacitor is no more than 33 pF and assuming 50 pF parasitic cap provides a good safety margin. We finally ended up using typical resistors and did not use a potentiometer in the testing process. The device sizing is summarized in table III.

In order to characterize the mismatch and process variations sensitivity, Monte-Carlo simulations has been performed on

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TABLE III
DESIGN EXAMPLE DEVICE SIZES: MULTIPLIER × (FINGERS × W) / L

Device	*Size*	*Device*	*Size*	*Device*	*Size*
M_{1a}	$6 \times (1 \times 7.5\mu m)/15\mu m$	M_{10}	$2 \times (1 \times 7.5\mu m)/15\mu m$	M_{5a}, M_{6a}	$2 \times (1 \times 7.5\mu m)/15\mu m$
M_{2a}	$2 \times (1 \times 7.5\mu m)/15\mu m$	M_{11}	$24\mu m/0.35\mu m$	M_{5b}, M_{6b}	$7.5\mu m/0.35\mu m$
M_{1b}, M_{2b}	$7.5\mu m/0.35\mu m$	M_{12}	$3\mu m/0.35\mu m$	M_7	$4\mu m/0.3\mu m$
M_{3b}, M_{4b}	$4\mu m/0.3\mu m$	M_{13b}, M_{14b}	$4\mu m/0.3\mu m$	M_8	$32\mu m/0.3\mu m$
M_{3a}, M_{4a}	$8 \times (1 \times 2.5\mu m)/15\mu m$	M_{13a}, M_{14a}	$8 \times (1 \times 2.5\mu m)/15\mu m$	M_9	$8 \times (1 \times 2.5\mu m)/15\mu m$
M_{res}	$0.22\mu m/4\mu m$	M_{s1}	$0.35\mu m/0.35\mu m$	M_{s3}	$4\mu m/0.35\mu m$
R	5742Ω	M_{s2}	$0.22\mu m/4\mu m$	M_{s4}	$4\mu m/0.35\mu m$

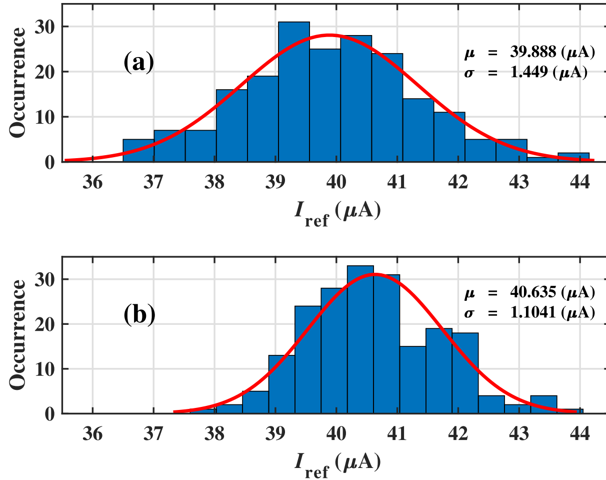

Fig. 6. Monte-Carlo simulation results: (a) split R implementation (b) the proposed structure.

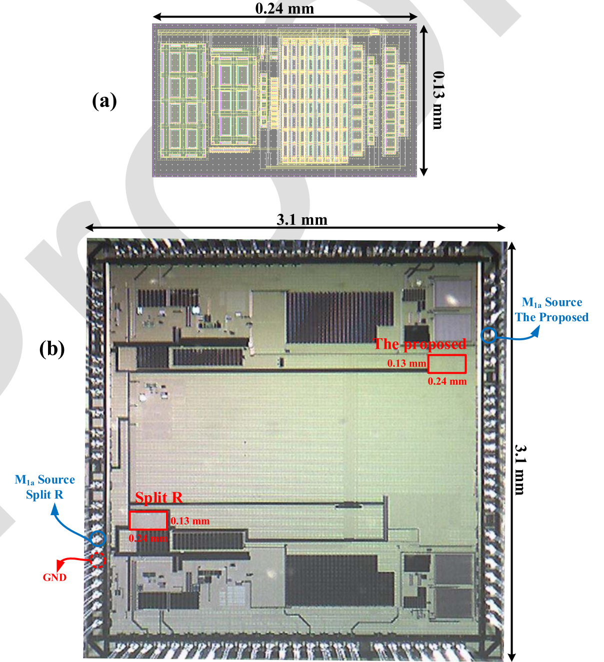

Fig. 7. The implementation (a) layout of the proposed reference current generator in 0.18 μm technology (b) the die micrograph of the fabricated chip.

the conventional split R and the proposed design. Figure 6a and 6 (b) show the results for 200 iterations. The proposed structure has lower dispersion compared to the split R which leads to 31% reduction in the standard deviation. Section V calculates a value of 25% which is close to the predicted value. The main reason for the mismatch can be the body effect of M_{1a}. This improvement is the result of removing the on-chip part of the resistor which results in higher precision.

VIII. MEASUREMENT RESULTS

Both the split R and the proposed structure were fabricated on the same chip in a 0.18 μm CMOS technology, each occupying an area of 0.13×0.24 mm^2. Figure 7a shows the layout implementation of the proposed structure. The layout for the conventional, split R structure has the same size with little differences.

The die micrograph is shown in Fig. 7b. The target reference current is 40.6 μA and measurement results of the sample chip show 42.1 μA for the split-R structure and 51.2 μA for the proposed structure. The source of this discrepancy is the physical distance between the proposed circuit and ground. Figure 7b shows the distance between the proposed circuit and ground is considerably higher than for the conventional one. Hence, the trace connecting proposed design to the ground produces a non-zero voltage due to its resistive voltage drop. In other words, the voltage of the ground connected to the bottom of R (Fig. 4) is still zero (because of the short distance) while all other grounds are connected to a biased ground with the voltage of some few millivolts. The voltage across R is now calculated as

$$V_R = V_{GND,2a} + V_{GS,2a} - V_{GS,1a} - V_{GND,R} \quad (41)$$

in which $V_{GND,2a}$ defines the voltage of the ground connected to the source of M_{2a} and $V_{GND,R}$ defines the voltage of the ground connected to the bottom of R. Consequently, the voltage across R is approximated to

$$V_R = V_{GS,2a} - V_{GS,1a} + V_{GND,2a}. \quad (42)$$

This V_R is higher than the designated voltage and increases the reference current produced by the proposed circuit. Simulations in the presence of a resistive voltage drop shows the proposed current bias generator will produce a current of 50.92 μA, which is close to the measured current of 51.2 μA. The conventional design is placed close to the chip ground and does not suffer this problem. This can be solved in a careful design which places the bias current generator block close to the chip ground or specifies a separate ground for it.

IX. CONCLUSION

A new proposed structure for implementing a constant g_m reference bias generator is presented that does minimum

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changes on the conventional circuit, keeps the structure stable and alleviates the sensitivity to the on-chip resistor deviations. This decreases the reference current deviations by 31% according to the simulation results. Implementation shows that the proposed structure is stable and provides a constant current.

FUTURE WORK

By removal of the on-chip resistor potion, purely Off-chip resistors with different temperature coefficients can be used which can provide a temperature-independent current or transconductance. Also, the proposed can be used for bandgap voltage or current references that are intended to be proportional to absolute temperature (PTAT) or complementary to absolute temperature (CTAT) or temperature independent by use of purely off-chip resistors with any desired thermal coefficient.

APPENDIX A
CALCULATIONS

A. Loop Gain Calculations

In order to calculate the loop gain, we use the T model of the MOSFET; this is a straightforward model especially for common-source transistors. The important thing is to make sure the current passing through the gate is zero. First, we calculate the small signal current going through the drain of M_1 (i_{ref}). The impedance connected to source of M_1 in Fig. 8 is calculated as

$$z' = \frac{rC(R-r)s + R}{C(R-r)s+1} \tag{43}$$

So, the impedance z (shown on Fig. 8 is calculated as:

$$\begin{aligned} z &= \frac{1}{g_{m1}} + z' = \frac{1}{g_{m1}} + \frac{rC(R-r)s+R}{C(R-r)s+1} \\ &= \frac{1}{g_{m1}} \cdot \frac{C(R-r)s + 1 + g_{m1}rC(R-r)s + g_{m1}R}{C(R-r)s+1} \end{aligned} \tag{44}$$

which can be simplified to

$$z = \frac{1}{g_{m1}} \cdot \frac{C(g_{m1}r+1)(R-r)s + g_{m1}R + 1}{C(R-r)s+1} \tag{45}$$

Assuming zero current going through the gate of M_1:

$$\begin{aligned} g_{m1}(v_g - v_s) &= \frac{v_s}{z'} => g_{m1}v_g = (g_{m1} + \frac{1}{z'})v_s => v_s \\ &= g_{m1}\frac{z'}{g_{m1}z'+1}v_g \end{aligned} \tag{46}$$

The v_{gs} is calculated as

$$v_{gs} = v_g - v_s = \frac{1}{g_{m1}} \cdot \frac{1}{z' + 1/g_{m1}}v_g \tag{47}$$

knowing v_g is equal to v_{in}, we can recalculate Eqn. 47:

$$v_{gs} = \frac{1}{g_{m1}} \cdot \frac{1}{z' + 1/g_{m1}}v_{in} \tag{48}$$

Looking at Fig. 8, the i_{ref} is produced by g_{m1} v_{gs}:

$$i_{ref} = g_{m1}v_{gs} = \frac{1}{z' + 1/g_{m1}}v_{in} = \frac{1}{z}v_{in} \tag{49}$$

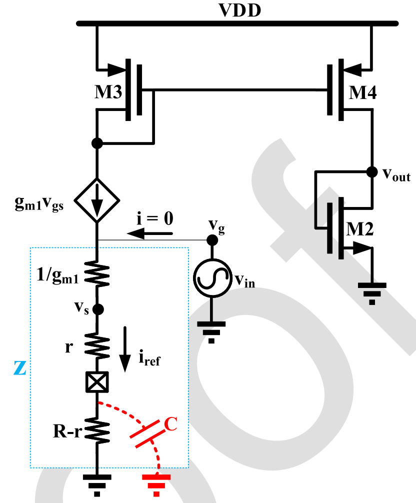

Fig. 8. Loop gain analysis equivalent circuit, we are using a T-Model of MOS no current should pass through the gate of M1.

This current is mirrored by M_3 and M_4 and goes to the output stage (M_2) which has a resistance of $1/g_{m2}$, it then produces the output voltage of

$$v_{out} = \frac{1}{g_{m2}} \cdot \frac{1}{z}v_{in} \tag{50}$$

The open loop gain is calculated as

$$\begin{aligned} A_v(s) &= \frac{v_{out}}{v_{in}} = \frac{1}{g_{m2}} \cdot \frac{1}{z}v_{in} \\ &= \frac{1}{g_{m2}} \times g_{m1}\frac{C(R-r)s+1}{C(g_{m1}r+1)(R-r)s + g_{m1}R + 1} \\ &= \frac{g_{m1}}{g_{m2}}\frac{C(R-r)s+1}{C(g_{m1}r+1)(R-r)s + g_{m1}R + 1} \end{aligned} \tag{51}$$

We know M_1 and M_2 carry the same current while M_1 is M times larger than M_2, so the first fraction in Eqn. 51 is equal to $\sqrt{M}$. We simplify the loop gain as

$$A_v(s) = \frac{\sqrt{M}}{g_{m1}R+1} \cdot \frac{C(R-r)s+1}{\frac{g_{m1}r+1}{g_{m1}R+1}C(R-r)s+1} \tag{52}$$

The high frequency loop gain is calculated as

$$A_v(\infty) = \frac{\sqrt{M}}{g_{m1}R+1} \cdot \frac{C(R-r)s}{\frac{g_{m1}r+1}{g_{m1}R+1}C(R-r)s} = \frac{\sqrt{M}}{g_{m1}r+1} \tag{53}$$

By substituting Eqn. 2 into Eqn. 52, we will have the loop gain

$$\begin{aligned} A_v(s) &= \frac{\sqrt{M}}{2(1-1/\sqrt{M})+1} \cdot \frac{C(R-r)s+1}{\frac{g_{m1}r+1}{g_{m1}R+1}C(R-r)s+1} \\ &= \frac{M}{3\sqrt{M}-2} \cdot \frac{C(R-r)s+1}{\frac{g_{m1}r+1}{g_{m1}R+1}C(R-r)s+1} \end{aligned} \tag{54}$$

Now, we calculate the high frequency loop gain (Eqn. 53) stability conditions by assuming the loop gain below unity:

$$\begin{aligned} A_v(\infty) < 1 &= > \frac{\sqrt{M}}{g_{m1}r+1} < 1 => \sqrt{M} < g_{m1}r+1 \\ &= > r > \frac{\sqrt{M}-1}{g_{m1}} \end{aligned} \tag{55}$$

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Substituting Eqn. 2 into Eqn. 55, we will have

$$r > \frac{\sqrt{M}-1}{\frac{2}{R}\left(1-\frac{1}{\sqrt{M}}\right)} => r > \frac{R}{2}\frac{\sqrt{M}-1}{\left(1-\frac{1}{\sqrt{M}}\right)} => r > \frac{R}{2}\sqrt{M} \tag{56}$$

B. Process Variations Calculations

With regard to sensitivity of $I_{\rm ref}$ to process variations on β and r, the following calculations will give us the standard deviations:

$$\sigma^2_{\frac{\Delta I_{\rm ref}}{I_{\rm ref}}}\bigg|_{\beta,\rm process} = \frac{A^2_{\beta,\rm process}}{W\times L}\left(\frac{\beta}{I_{\rm ref}}\cdot\frac{\partial I_{\rm ref}}{\partial\beta}\right)^2 = \frac{A^2_{\beta,\rm process}}{W\times L} \tag{57}$$

$$\Delta I_{\rm ref} = \Delta R\frac{\partial I_{\rm ref}}{\partial R} = \frac{\Delta R}{R}(-2I_{\rm ref}). \tag{58}$$

So,

$$\frac{\Delta I_{\rm ref}}{I_{\rm ref}} = -2\frac{\Delta R}{R} \tag{59}$$

For the split R structure (Fig. 1a), just the on-chip portion is changing with the process so

$$R = (R-r)_{\rm off-chip} + r => \Delta R = \Delta r \tag{60}$$

so we can rewrite the equation:

$$\frac{\Delta I_{\rm ref}}{I_{\rm ref}} = -2\frac{\Delta R}{R} = -2\frac{\Delta r}{r}\cdot\frac{r}{R}. \tag{61}$$

Now, we can calculate the normalized standard deviation:

$$\sigma_{\frac{\Delta I_{\rm ref}}{I_{\rm ref}}}\bigg|_{\rm r,process} = \sigma_{\frac{\Delta r}{r}}\left(2\frac{r}{R}\right) = \left(\frac{A_{\rm r,process}}{W}\right)\cdot\left(2\frac{r}{R}\right) \tag{62}$$

C. Mismatch Calculations

Looking at Fig. 1b

$$V_{\rm GS2} = V_{\rm GS1} + RI_{\rm ref}. \tag{63}$$

$$\frac{\beta_1 M}{2}(V_{\rm GS1}-V_{\rm th1})^2 = \frac{\beta_2}{2}(V_{\rm GS2}-V_{\rm th2})^2 => V_{\rm GS2} = V_{\rm th2} + \sqrt{\frac{\beta_1 M}{2}}(V_{\rm GS1}-V_{\rm th1}) \tag{64}$$

Substituting Eqn. 64 into Eqn. 63

$$RI_{\rm ref} = V_{\rm th2} - V_{\rm th1}\sqrt{\frac{\beta_1 M}{\beta_2}} + \left(\sqrt{\frac{\beta_1 M}{\beta_2}}-1\right)V_{\rm GS1} \tag{65}$$

Square law for the transistor:

$$I_{\rm ref} = \frac{\beta_1 M}{2}(V_{\rm GS1}-V_{\rm th1})^2 => V_{\rm GS1} = V_{\rm th1} + \sqrt{\frac{2I_{\rm ref}}{\beta_1 M}} \tag{66}$$

Substituting Eqn. 66 in Eqn. 65

$$RI_{\rm ref} = V_{\rm th2} - V_{\rm th1} + \sqrt{\frac{2I_{\rm ref}}{\beta_2}} - \sqrt{\frac{2I_{\rm ref}}{\beta_1 M}} \tag{67}$$

$$I_{\rm ref} = x^2 \tag{68}$$

$$Rx^2 - \left(\sqrt{\frac{2}{\beta_2}} - \sqrt{\frac{2}{\beta_1 M}}\right)x + (V_{\rm th1}-V_{\rm th2}) = 0 \tag{69}$$

Solving the second order equation:

$$\Delta = \left(\sqrt{\frac{2}{\beta_2}} - \sqrt{\frac{2}{\beta_1 M}}\right)^2 - 4R(V_{\rm th1}-V_{\rm th2}) \tag{70}$$

The non-zero root is

$$x_2 = \frac{\sqrt{\frac{2}{\beta_2}} - \sqrt{\frac{2}{\beta_1 M}} + \sqrt{\left(\sqrt{\frac{2}{\beta_2}} - \sqrt{\frac{2}{\beta_1 M}}\right)^2 - 4R(V_{\rm th1}-V_{\rm th2})}}{2R} \tag{71}$$

Using Eqn. 68

$$I_{\rm ref} = (x_2)^2 = \frac{1}{4R^2}\left(\left(\sqrt{\frac{2}{\beta_2}} - \sqrt{\frac{2}{\beta_1 M}}\right) + \sqrt{\left(\sqrt{\frac{2}{\beta_2}} - \sqrt{\frac{2}{\beta_1 M}}\right)^2 - 4R(V_{\rm th1}-V_{\rm th2})}\right)^2 \tag{72}$$

Now, we can calculated the derivatives:

$$\Delta I_{\rm ref} = \Delta\beta\frac{\partial I_{\rm ref}}{\partial\beta_1} + \Delta\beta\frac{\partial I_{\rm ref}}{\partial\beta_2} + \Delta V_{\rm th}\frac{\partial I_{\rm ref}}{\partial V_{\rm th1}} + \Delta V_{\rm th}\frac{\partial I_{\rm ref}}{\partial V_{\rm th2}} \tag{73}$$

Now, if we divide both sides by $I_{\rm ref}$ and rearranging the formula

$$\frac{\Delta I_{\rm ref}}{I_{\rm ref}} = \frac{\Delta\beta}{\beta_1}\left(\frac{\beta_1}{I_{\rm ref}}\cdot\frac{\partial I_{\rm ref}}{\partial\beta_1}\right) + \frac{\Delta\beta}{\beta_2}\left(\frac{\beta_2}{I_{\rm ref}}\cdot\frac{\partial I_{\rm ref}}{\partial\beta_1}\right) + \frac{\Delta V_{\rm th}}{I_{\rm ref}}\frac{\partial I_{\rm ref}}{\partial V_{\rm th1}} + \frac{\Delta V_{\rm th}}{I_{\rm ref}}\frac{\partial I_{\rm ref}}{\partial V_{\rm th2}} \tag{74}$$

Now, if we calculate the variance

$$\sigma^2_{\frac{\Delta I_{\rm ref}}{I_{\rm ref}}} = \sigma^2_{\frac{\Delta\beta 1}{\beta}}\left(\frac{\beta_1}{I_{\rm ref}}\cdot\frac{\partial I_{\rm ref}}{\partial\beta_1}\right)^2 + \sigma^2_{\frac{\Delta\beta 2}{\beta}}\left(\frac{\beta_2}{I_{\rm ref}}\cdot\frac{\partial I_{\rm ref}}{\partial\beta_2}\right)^2 + \sigma^2_{\Delta V_{\rm th1}}\left(\frac{1}{I_{\rm ref}}\frac{\partial I_{\rm ref}}{\partial V_{\rm th1}}\right)^2 + \sigma^2_{\Delta V_{\rm th2}}\left(\frac{1}{I_{\rm ref}}\frac{\partial I_{\rm ref}}{\partial V_{\rm th2}}\right)^2 \tag{75}$$

The $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\rm Vth}$ are

$$\sigma_{\frac{\Delta\beta 1}{\beta}} = \frac{A_\beta}{\sqrt{M\times W\times L}},\quad \sigma_{\frac{\Delta\beta 2}{\beta}} = \frac{A_\beta}{\sqrt{W\times L}} \tag{76}$$

$$\sigma_{\Delta V_{\rm th1}} = \frac{A_{\rm Vth}}{\sqrt{M\times W\times L}},\quad \sigma_{\Delta V_{\rm th2}} = \frac{A_{\rm Vth}}{\sqrt{W\times L}} \tag{77}$$

So, we can rewrite relation 75:

$$\sigma^2_{\frac{\Delta I_{\rm ref}}{I_{\rm ref}}} = \frac{A^2_\beta}{W\times L}\left(\frac{1}{M}\cdot\left(\frac{\beta_1}{I_{\rm ref}}\cdot\frac{\partial I_{\rm ref}}{\partial\beta_1}\right)^2 + \left(\frac{\beta_2}{I_{\rm ref}}\cdot\frac{\partial I_{\rm ref}}{\partial\beta_2}\right)^2\right) + \frac{A^2_{\rm Vth}}{W\times L}\left(\frac{1}{M}\cdot\left(\frac{1}{I_{\rm ref}}\frac{\partial I_{\rm ref}}{\partial V_{\rm th1}}\right)^2 + \left(\frac{1}{I_{\rm ref}}\frac{\partial I_{\rm ref}}{\partial V_{\rm th2}}\right)^2\right) \tag{78}$$

$$\frac{\beta_1}{I_{\rm ref}}\cdot\frac{\partial I_{\rm ref}}{\partial\beta_1} = \bigg|_{\beta_1=\beta_2,V_{\rm th1}=V_{\rm th2}} = \frac{1}{\sqrt{M}-1} \tag{79}$$

$$\frac{\beta_2}{I_{\rm ref}}\cdot\frac{\partial I_{\rm ref}}{\partial\beta_2}\bigg|_{\beta_1=\beta_2,V_{\rm th1}=V_{\rm th2}} = -\frac{\sqrt{M}}{\sqrt{M}-1} \tag{80}$$

$$\frac{1}{I_{\rm ref}}\cdot\frac{\partial V_{\rm ref}}{\partial V_{\rm th1}}\bigg|_{\beta_1=\beta_2,V_{\rm th1}=V_{\rm th2}} = -\frac{M\beta R}{\left(\sqrt{M}-1\right)^2} \tag{81}$$

$$\frac{1}{I_{\rm ref}}\cdot\frac{\partial V_{\rm ref}}{\partial V_{\rm th2}}\bigg|_{\beta_1=\beta_2,V_{\rm th1}=V_{\rm th2}} = \frac{M\beta R}{\left(\sqrt{M}-1\right)^2} \tag{82}$$

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611 We can re-write the Eqn. 78:

$$\sigma^2_{\frac{\Delta I_{\text{ref}}}{I_{\text{ref}}}} = \frac{A^2_\beta}{W \times L} \cdot \frac{M + 1/M}{\left(\sqrt{M} - 1\right)^2} + \frac{A^2_{\text{Vth}}}{W \times L} \cdot \frac{(M^2 + M)(\beta R)^2}{\left(\sqrt{M} - 1\right)^4} \tag{83}$$

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