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A CMOS monolithic amplifier for cardiac EIT applications

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Abstract
A wide bandwidth amplifier for cardiac electrical impedance tomography applications is presented with detailed analysis. To minimize mismatch, we employ a balanced architecture that is symmetric without systematic offset. Our low-complexity design is suitable for broadband operation and for rejecting high-frequency common-mode interference. A prototype chip was designed and fabricated in a 180 nm CMOS process to demonstrate the performance of the proposed amplifier. The amplifier operates over a bandwidth of 6 MHz, and attenuates common-mode interference by −74 dB at 2 MHz. Measured total harmonic distortion is −62 dB at 100 kHz, and the spurious-free dynamic range is 71 dB.

Keywords Instrumentation amplifier (IA) · CMOS · Bioimpedance application · Medical applications · High CMRR · Electrical impedance tomography (EIT) · Preamplifier

1 Introduction

Heart failure patients can improve their self-management by continuously monitoring their cardiac hemodynamics [12, 17, 35, 39, 58, 63]. To this end, electrical impedance tomography (EIT) is a promising technology that can provide non-invasive monitoring of pulmonary artery pressure [50], fluid overload [34], and other signs of hemodynamic status.

Figure 1 is a simplified diagram of a multi-channel cardiac EIT system. Current drivers inject small alternating currents to the thorax, following the IEC 60601-1 compliance requirements [38], and the resulting surface electric potentials are measured with a phase-sensitive voltmeter. Multiplexers allow each channel to be used either for current injection or for voltage readout.

The first stage of the voltage readout chain is an AC-coupled instrumentation amplifier (IA), which blocks electrode offsets [36, 47, 54, 71] and provides initial amplification. To meet the requirements of cardiac EIT, the AC-coupled IA must reject 1 V_{pp} common mode interference in the range of 100 Hz to 1 MHz [46, 52, 55]. It must also provide a 65 dB spurious-free dynamic range (SFDR) based on a 333 μV_{rms} input referred voltage noise and a THD of −40 dB [11, 19, 22, 52]. For a wearable system, the IA must meet these performance specifications while consuming a minimal amount of power. Unfortunately, there are currently no solutions that meet all of these challenges. For example, commercial amplifiers used in conventional EIT systems [44, 45, 66, 72] are unsuitable for a wearable solution, because they consume too much power. Furthermore, amplifier designs from the state-of-the-art ASICs either require tunable capacitors [67] or precisely-matched gain elements [25] to maintain the overall common-mode performance. Also they do not meet the input dynamic range requirement.

In this paper, we present a CMOS amplifier that is suitable for an EIT instrumentation system that targets wearable cardiac applications. The proposed amplifier has a balanced structure and an active common-mode feedback circuit that can reject 1 V_{pp} common mode interference at frequencies up to 4 MHz without relying on post-fabrication tuning. Further, it can process input signals up to a 0.667 V_{pp} swing with <−50 dB THD, and consumes less than 1 mA of current.

2 Amplifier performance requirements

Beyond the analog front-end shown in Fig. 1, a cardiac EIT system consists of several components, including a digital block for matched filtering, an FPGA for control and

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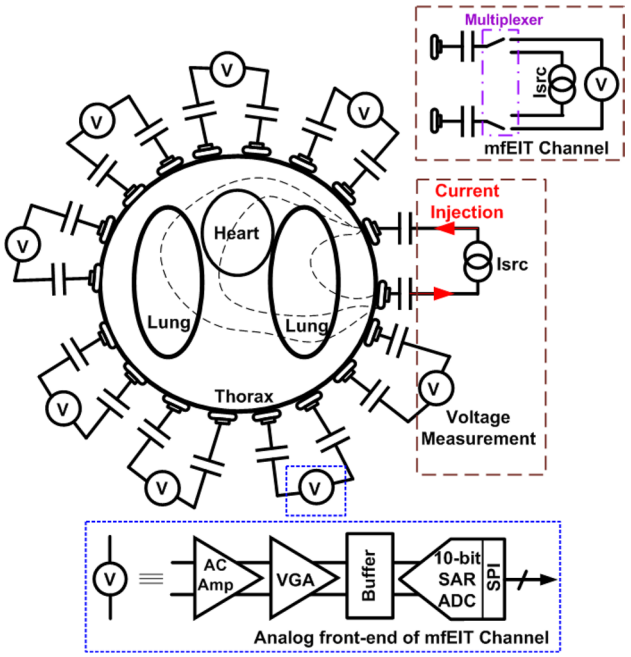

Fig. 1 Simplified multi-channel EIT system for cardiac applications

communication, and a reconstruction algorithm to obtain the final image of the thorax. We are in the process of building and evaluating a complete EIT system that is based on our custom integrated circuit analog front-end. However, this paper aims to isolate and measure the performance of the instrumentation amplifier alone, without it being confounded by other components of the EIT system.

To this end, we have derived the performance requirements of our amplifier from computational experiments that we performed on a highly-detailed digital phantom of the human thorax that was developed at Dartmouth College [6, 41]. The digital phantom comprises the MRI and CT-based 4D XCAT model [57], mesh generation using distmesh [49] and gmsh [16], a perfusion model [8], ex-vivo tissue values of conductivity and permittivity from multiple frequencies [5], and a 3D finite element (FEM) implementation of the complete electrode [7]. Thoracic digital phantoms have been validated and used extensively for research in several biomedical imaging modalities [3, 9, 37, 40, 48], including electrical impedance tomography [41].

EIT imaging involves phase-sensitive measurement of *boundary voltages*. These are voltages that develop on the surface of the tissue as a result of the injected current and the internal conductivity distribution of the tissue. We have used the digital phantom to study the boundary voltage amplitudes that are generated at a typical electrode position, with measurements taken across the cardiac cycle. Depending on the anatomy of the subject, the boundary voltages can range in amplitude from tens of millivolts to several hundred millivolts [52] when a 5 mA, 1 MHz interrogation current is applied to the thorax. So, assuming an ADC input range of 1 V, the IA must provide a gain of approximately 3 V/V. The variable gain amplifier that follows the IA (see Fig. 1) can provide more gain if necessary.

The frequency of the injected current (and hence that of the boundary voltages) that is used in cardiac EIT can range from 100 Hz to 1 MHz. The higher interrogation frequencies are needed in applications such as measuring fluid index ratio in congestive heart failure [34], detecting cardiac ischemia [15], and characterizing anatomic features [2]. To be useful across all these applications, the IA must operate over the frequency range 100 Hz to 1 MHz.

EIT systems experience common mode interference that is at the same frequency as the injected current (and differential boundary voltages) [23, 51, 67]. As shown in Figs. 2 and 3, both the injected current I_{inject} (Fig. 2) and the residual (mismatch) current between differential current sources (Fig. 3) will flow through a low impedance path back to its source. Therefore, the AC common-mode signal (mean body voltage [55]) at the amplifier inputs can be as large as 1 V_{pp} as a result of a 10 mA_{pp} return

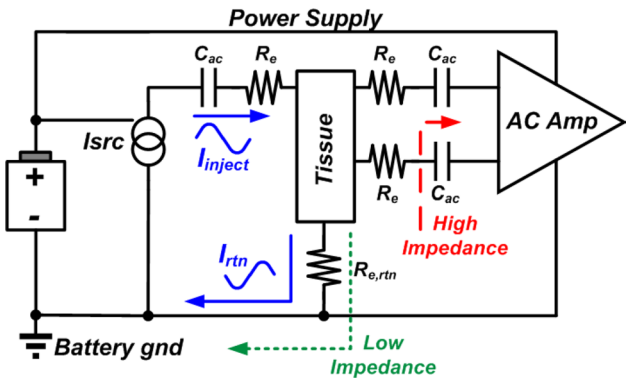

Fig. 2 Simplified EIT measurement channel with a single-ended current injection (Isrc) and a differential voltage sensing

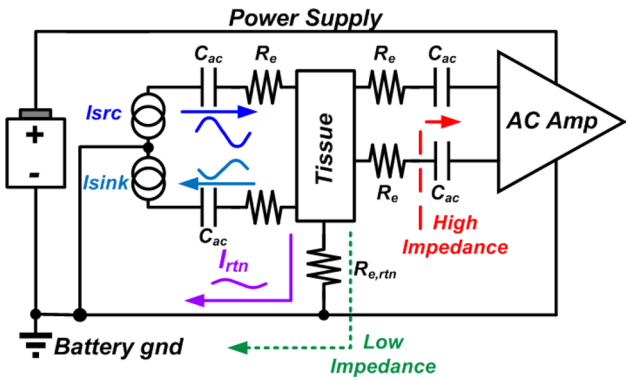

Fig. 3 Simplified EIT measurement channel with a differential current source (Isrc, Isink) and a differential voltage sensing setup

current flowing through a 100 Ω $R_{e,rm}$ contact impedance (100 Ω is typical for the type of dry electrodes that are suitable for ambulatory EIT applications [43]). The common-mode signal cannot be suppressed with a driven right leg circuit, as this creates stability problems when applied to high frequency applications [18, 55]. Instead, the analog read-out chain must provide adequate common mode rejection ratio (CMRR) performance. Research studies have shown that for a system error of 1 %, a CMRR of 70 dB is required for the amplifier [47, 55]. Assuming an electrode and channel multiplexer CMRR of 80–90 dB, the instrumentation amplifier must provide a CMRR of 80 dB, across the entire working frequency of 100 Hz to 1 MHz [46, 55]. Note, electrode offset is not a concern in EIT systems, because a 1 μF DC blocking capacitor is placed between the electrodes and the read-out chain for patient safety [52].

In addition to its bandwidth and common-mode rejection requirements, the amplifier must provide adequate noise performance to meet the EIT system signal-to-noise ratio (SNR) specification. The poorly conditioned, ill-posed nature of EIT image reconstruction demands a system-level SNR of 80 dB [41]. To achieve this, the output referred noise ("referred to output", RTO) of the amplifier must be less than 1 m$V_{\rm rms}$ (333 $\mu V_{\rm rms}$, input referred) [42, 52]. Linearity requirements are less stringently defined, especially with the use of the calibration techniques that we introduced in [19]. Still, it is typical to design for 40 dB total harmonic distortion [11, 19, 22].

For a wearable cardiac EIT system design for ambulatory care or telemonitoring applications, system power consumption must be minimized. This is necessary for patient comfort (by obviating the need for a wall plug in, and reducing the size of the battery), as well as for patient safety with regard to heating. Cutting-edge ASIC-based wearable EIT systems consume less than 6 nW/electrode·Hz [24, 25, 32], which leads to 6 mW/electrode for a 1 MHz EIT system. The power consumption break down for a custom ASIC that targets cardiac EIT application are as follows: instrumentation amplifier (2.07 mW), variable gain amplifier (4.66 mW), current driver (1.65 mW), ADC (139 µW) [52]. The digital matched filter will consume on the order of 0.7 mW/channel [26, 69]. The transmission of the amplitude and phase data will consume roughly < 1 mW [59]. In our application, multiplexers consist of passive switches, and do not consume an appreciable amount of power. From the above power budget, the instrumentation amplifier and variable gain amplifier are the primary consumers of power to satisfy the high-speed and high dynamic range requirements. The amplifier should reduce the power burden of the overall EIT system, and consume less than 1 mA using a 3.3 V power supply.

3 State-of-the-art approaches

To the best of our knowledge, none of the previously-existing solutions meet our design and power specifications.

For example, a commercial off-the shelf differential receiver amplifier like the AD8130 provides low signal distortion, wide voltage swings and a high CMRR at high frequencies. However, it is a general-purpose design that dissipates at least 50 mW.

A low power instrumentation amplifier (IA) based on the current feedback structure was reported to provide an average 90 dB CMRR at 2 MHz [67], but it has an imbalanced structure and requires tunable capacitors (varactors) to neutralize the systematic mismatch at high frequencies. Also it does not meet our differential output swing requirement.

The popular capacitive-feedback amplifier utilized in low frequency biopotential acquisition systems [21] can be adopted for an EIT system, which can provides 90 dB CMRR with an 18 dB voltage gain [25]. Even so, from the case study of [1], the effect of capacitance mismatch dominates the input common-mode performance of the feedback amplifier for an input frequency larger than 1 Hz. The mid-band common-mode gain of the amplifier is −40 dB for a 1% mismatch on capacitors. Therefore, precisely matched capacitors [4] are required to achieve a common-mode gain of −72 dB reported in [25]. Based on our available CMOS technology and the broadband operation requirement, a high power feedback amplifier is required to drive large-value gain capacitors which sized for a mismatch less than 0.026 %. That is to say, it demands a less than 5 fF mismatch between two 20 pF capacitors. As a result, it could be a challenge to implement a monolithic amplifier based on the feedback amplifier architecture to have a common-mode gain $A_{\rm v,CM} < -70$ dB.

4 Proposed amplifier

4.1 Overview of architecture

The amplifier is based on the universal current conveyor instrumentation amplifier (UIA) [65], which comprises two class II current conveyors (CCII) and resistors (Fig. 4). As Fig. 4 illustrates, an ideal CCII provides high input impedance at node Y, current buffering ($I_z = I_x$) and voltage buffering ($V_x = V_y$). These features are used in concert with two resistors, R_1, R_2, to realize an instrumentation amplifier with a gain of R_2/R_1. With high input impedance, easy gain adjustments and inherent large common-mode rejection capability, the UIA is a popular structure

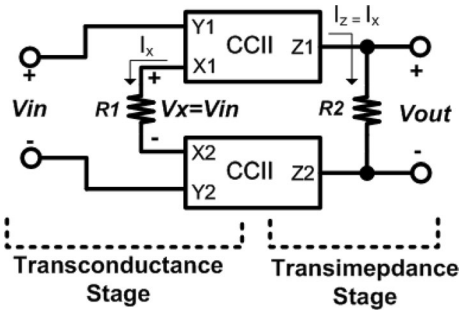

Fig. 4 Universal current conveyor instrumentation amplifier

for biopotential acquisition systems used for EEG, ECG and EIT measurements [64, 67, 71].

Figure 5 shows the schematic diagram of the proposed amplifier. It consists of a transconductance stage, a transimpedance stage and an output stage. The transconductance stage converts input voltages into a signal current V_{in}/R_1, and this signal current is transmitted from the transconductance stage to transimpedance stage to produce a signal voltage across R_2. Thus, the gain of the amplifier is R_2/R_1.

The transconductance stage is implemented as a symmetric structure with two level-shifted g_m-boosted flipped source followers (transistor M_1-M_4) and a resistor R_1. The current boosting action, provided by transistor M_3 and $M_{3'}$, reduces the source node impedance of input transistors M_1, $M_{1'}$. This is crucial for driving low values of R_1, which is necessary for achieving low noise operation (see Sect. 4.4). Figure 6 shows the half circuit low frequency differential small signal model of the amplifier. The voltage gain from input to the source of M_1 is given by:

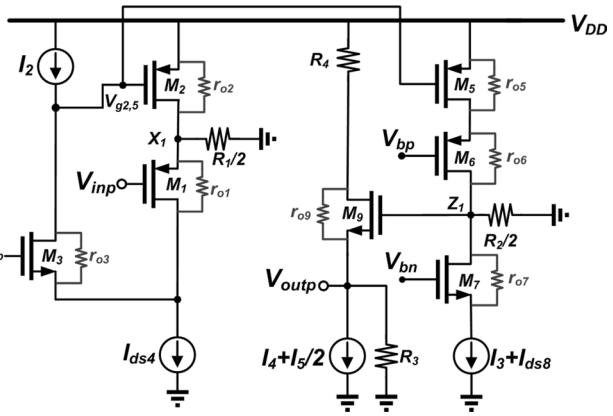

Fig. 6 Simplified small signal half circuit model of the amplifier for the gain analysis

$$\frac{V_{X_1}}{V_{\text{inp}}} \approx \frac{1}{1+\frac{2}{g_{m1}r_{o1}g_{m2}R_1g_{m3}r_{o3}}} \approx 1, \tag{1}$$

and an output impedance $R_{\text{out}} \approx 1/(g_{m1}r_{o1}g_{m2}g_{m3}r_{o3})$, where g_{mx} and r_{ox} are the transconductance and the output resistance of transistor M_x.

The transimpedance stage consists of two PMOS cascode amplifiers, each with its own NMOS cascode load that operates as a current source, and a resistor R_2 connected between their outputs [64]. The transimpedance stage expands compressed AC voltages at node V_{g2} and $V_{g2'}$. Voltages at V_{g2} and $V_{g2'}$ in Fig. 5 are used to create the CCII's current mirroring characteristic between terminals X and Z of Fig. 4, which includes transistor M_2, $M_{2'}$ in the transconductance stage and M_5, $M_{5'}$ in the transimpedance stage. The NMOS

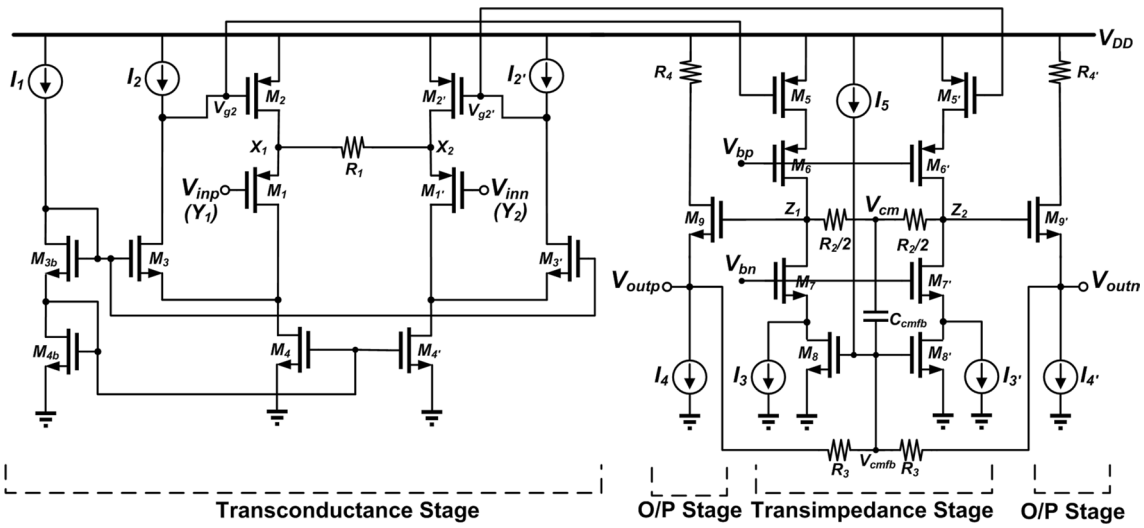

Fig. 5 Schematic diagram of the amplifier using balanced structure in each stage

current sources (M_8, $M_{8'}$, I_3, $I_{3'}$) force the AC signal current from transistors M_5, $M_{5'}$ to flow through R_2 to generate the output voltage.

The voltage gain of the amplifier can be found by using the small signal half circuit [53] shown in Fig. 6. The low-frequency voltage gain can be expressed as

$$\begin{aligned}\frac{V_{\text{outp}}}{V_{\text{inp}}} &= \frac{V_{g2,5}}{V_{\text{inp}}} \times \frac{V_{Z1}}{V_{g2,5}} \times \frac{V_{\text{outp}}}{V_{Z1}} \\ &\approx \frac{-1}{g_{m2}(r_{o2} \parallel R_1/2) + (g_{m1} r_{o1} g_{m3} r_{o3})^{-1}} \\ &\quad \times (-g_{m5}\frac{R_2}{2}) \times \frac{1}{1 + (g_{m9} r_{o9})^{-1} + \frac{r_{o9}+R_4}{g_{m9} r_{o9} R_3}} \\ &\approx \frac{R_2}{R_1},\end{aligned} \tag{2}$$

for $r_{o2} \gg R_2/2$, $g_{m2} = g_{m5}$ and $g_{mx} r_{ox} \gg 1$. The amplifier's input voltages can range from tens to hundreds of mV [52]. Therefore, we designed the voltage gain of the amplifier to be 3 (V/V). Additional voltage gain can be provided by the VGA in the read-out channel (Fig. 1).

4.2 Wide bandwidth operation

A voltage buffer is required to implement the voltage transfer from the node Y to node X in Fig. 4. For general use, a voltage buffer would based on an operational amplifier configured in unity-gain feedback. Unfortunately, that approach is not suitable for our low-power, high speed requirements. For a wide bandwidth operation, the voltage buffer needs to reduce its internal high-impedance node. To this end, the level-shifted flipped source follower in Fig. 5 has the benefits of a simple architecture and wide bandwidth operation. By making the pole associated with the gate of M_2 dominate (Fig. 5), the feedback loop formed by transistor M_1, M_2 and M_3 has a loop bandwidth of 8 MHz and a loop phase margin (PM) close to 90°.

A low power output stage [33, 62] is used after the transimpedance stage to prevent the amplifier's bandwidth from being set (and limited) by R_2 and large output loading capacitors. Resistor R_4 and $R_{4'}$ are used for level shifting the output source followers.

4.3 High frequency common-mode rejection

Following the approach described in [53], the common-mode response ($A_{\text{v,CM}}$) of the amplifier in Fig. 5 can be found by first assuming the circuit is symmetric. Then, shorting like nodes together and combining transistors and current sources, the amplifier small signal circuit can be reduced to that depicted in Fig. 7. The capacitor C_{cmfb} allows node V_{cmfb} to track V_{CM} with a DC level shift. Under

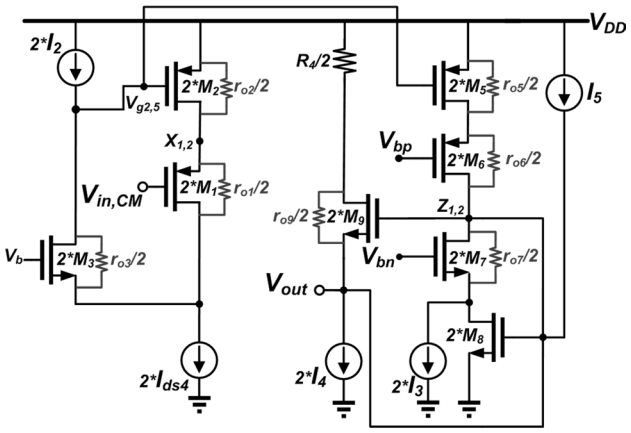

Fig. 7 Simplified equivalent circuit of the amplifier for the common-mode analysis

quiescent conditions, the quiescent current is set by the voltage at node V_{cmfb}. Under dynamic conditions, AC common-mode signal variations at node V_{CM} are passed to node V_{cmfb}. Therefore, we shorted the gate of M_8 and the drain of M_7 in Fig. 7 for common-gain analysis. The common-mode gain of the amplifier is equal to:

$$\begin{aligned}A_{\text{v,CM}} &= \frac{V_{out}}{V_{in,CM}} \\ &\approx \frac{-1}{g_{m2} r_{o2} + (g_{m1} r_{o1} g_{m3} r_{o3})^{-1}} \times \frac{-g_{m5}}{g_{m8}} \times 1 \\ &\approx \frac{g_{m5}}{g_{m2} r_{o2} g_{m8}} \approx \frac{1}{g_{m8} r_{o2}}.\end{aligned} \tag{3}$$

Based on Eq. 3, the transconductance stage suppresses an input common-mode interference by $g_{m2} r_{o2}$, which is reduced by a further g_{m5}/g_{m8} in the transimpedance stage. If the amplifier is perfectly symmetric, then both branches of the circuit would attenuate the common mode signal by exactly $g_{m8} r_{o2}$, where the common-mode to differential-mode gain ($A_{\text{CM–DM}}$) would be 0 (V/V).

The common-mode performance of the amplifier is, in practice, limited by the mismatch between nominally symmetric branches. Also, parasitic paths from the layout implementation degrade the high-frequency common-mode performance of the amplifier. Assume that the circuit is symmetric, except that transistors M_5 and $M_{5'}$ suffer from a gm mismatch of Δg_{m5}. Neglecting the capacitance at node V_{g2}, $V_{g2'}$, we have $|A_{\text{CM–DM}}| = \Delta g_{m5} V_{g2} R_2$. Chopper modulation and dynamic element matching can suppress the mismatch of the amplifier [13, 54, 67]. However, these techniques require high frequency clocks and additional filters, which makes them unsuitable for a wide bandwidth continuous-time amplifier.

In our amplifier, we achieve common mode rejection through the careful layout and choice of transimpedance

architecture. The transistors that are critical for common mode rejection, $M_{5,5'}$ and $M_{8,8'}$, are laid out in a common-centroid pattern. Moreover, the architecture of the transimpedance stage is chosen for its simple feedforward path, which limits the number of internal nodes and parasitic elements.

4.4 Low noise design

The schematic of Fig. 8 is the equivalent circuit model of the amplifier used to calculate the total input referred voltage noise power spectral density (PSD), and can be expressed as

$$\begin{aligned}\overline{V_{n,in}^2} \approx & 2\overline{V_{M1}^2} + \overline{V_{R1}^2} + 2g_{m2}^2R_1^2r_{op}^2\left(\overline{V_{M4}^2}g_{m4}^2\right. \\ & \left. + \overline{V_{M3}^2}g_{m3}^2 + \overline{V_{Mp}^2}g_{mp}^2\right) + 4\overline{V_{M2}^2}g_{m2}^2R_1^2 \\ & + \left[\frac{2(\overline{I_4^2} + \overline{I_{R3}^2} + \overline{I_{R4}^2})g_{m9}^{-2} + 2\overline{V_{M9}^2} + \overline{V_{R2}^2}}{R_2^2}\right. \\ & \left. + \overline{V_{M8}^2}g_{m8}^2\right]R_1^2,\end{aligned} \tag{4}$$

where $\overline{V_{Mx}^2}$, $\overline{I_x^2}$, g_{mx} and R_{out} are input referred voltage noise PSD, current noise PSD, small signal transconductance of transistor M_x, and the output impedance at node X, respectively. Following the Eq. 4, we designed the amplifier such that the total noise contribution due to new g_m-boosted devices and low value R_1 is lower than a high value R_1 alone. From Eq. 4, the contribution of R_1, V_{M8}^2 and V_{M2}^2 to the total noise can be large because of the multiplication of $g_{m2}^2R_1^2$ and $g_{m8}^2R_1^2$. The noise and the power consumption can be optimized by reducing the value of R_1 and sizing the input transistors M_1 and $M_{1'}$ to have large transconductances relative to the other transistors. The lower limit of the resistance of R_1 is set by:

$$\frac{1}{\frac{R_1}{2}g_{m1}r_{o1}g_{m2}g_{m3}r_{o3}} \ll 1, \tag{5}$$

which can be derived from Eq. 1. To target a total output noise less than 1 mV_{rms} and a bandwidth of integration of 100 MHz, the input-referred noise spectral density ("referred to input", RTI) must be less than 33 nV$rms/\sqrt{Hz}$. Based on Eqs. 4 and 5, and considering the input voltage range and the power budgets, the resistor R_1 is set to 10 kΩ where g_{m1} = 1 mS. From Eq. 4, the input-referred total integrated noise of the amplifier is 181 μV_{rms}, which corresponds to an input-referred voltage spectral density of 18 nV$rms/\sqrt{Hz}$.

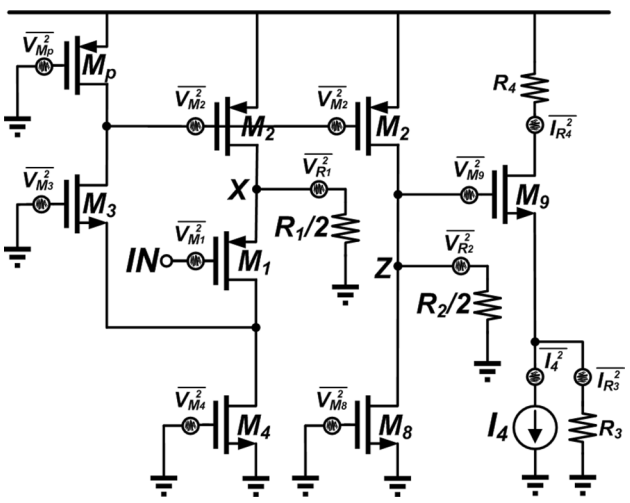

Fig. 8 Circuit model of the amplifier for the noise analysis

4.5 Wide dynamic range input stage

As previously detailed, the level-shifted flipped source follower is used as a voltage buffer in the transconductance stage in Fig. 5. Compared to the simple source follower, the flipped source follower (Fig. 9(a)) and the super source follower (Fig. 9(b)), the level-shifted flipped source follower has a lower output impedance of $R_{\text{out}} \approx 1/(g_{m1}r_{o1}g_{m2}r_{o2}g_{m3})$. Furthermore, the level shifting blocks in the feedback path using a transistorM_3 (Fig. 9(c)) [27, 29] or a resistor [30] solve the problem of limited input voltage range that is encountered in the flipped source follower design.

Furthermore, a feedback loop not only reduces the output impedance of the level-shifted flipped source follower (Fig. 9(a)), but it also improves its linearity. Figure 10 shows the simplified half circuit model of the level-shifted flipped source follower for linearity evaluation. Assuming current source I_1 is ideal, the small signal currents flowing through transistor M_1 and M_2 will be zero, and can be expressed as

$$\delta I_{d1} = 0 = g_{m1}(\delta V_{\text{out}} - \delta V_{\text{in}}) + \frac{\delta V_{d1} - \delta V_{\text{out}}}{r_{o1}} \tag{6a}$$

$$\delta I_{d2} = 0 = \frac{\delta V_{\text{out}}}{r_{o2}} - \delta V_{g2}g_{m2}, \tag{6b}$$

where δV_{dx}, δV_{gx}, and δI_{dx} represent small signal voltage and current changes of a transistor M_x, and δV_x is the small signal voltage change of node x. From Eq. 6a and assuming $g_{m1}r_{o1} \gg 1$, the small signal change at the output node with respect to the change of input is

$$\frac{\delta V_{\text{out}}}{\delta V_{\text{in}}} \approx \frac{g_{m1}r_{o1}g_{m2}r_{o2}A}{1 + g_{m1}r_{o1}g_{m2}r_{o2}A}, \tag{7}$$

where the amplifier A represents the small signal gain between nodes V_{d1} and V_{g2}. Equation 7 shows that V_{out} closely tracks the change in V_{in}, and is insensitive to changes

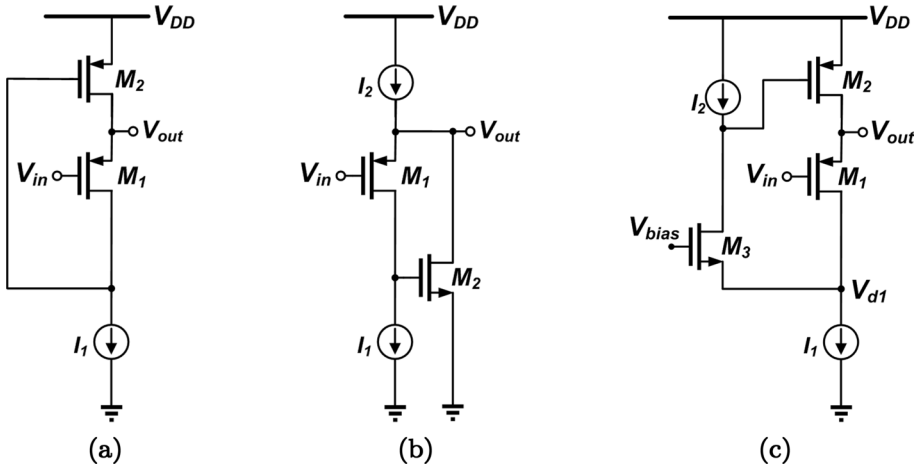

Fig. 9 **a** Flipped source follower. **b** Super source follower. **c** Flipped source follower with transistor M_3 as a level shifter [29]

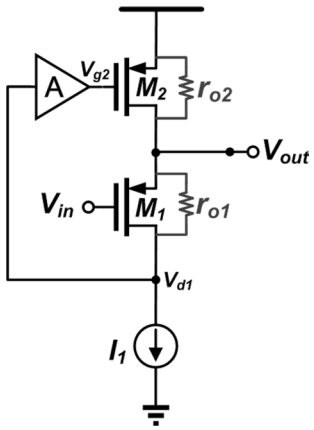

Fig. 10 Simplified schematic of the level-shifted flipped source follower for linearity evaluation. The amplifier **A** represents the gain of the common-gate stage M_2 in Fig. 9(c)

in g_m and r_o that are due to a large input signal. Moreover, the feedback loop (Fig 10) reduces the change at node V_{d1} by a factor of A; this reduces the effect of current source I_1's finite output impedance [61, 62]. More formal IIP3 and P1dB analyses would yield similar conclusions, but the amplifier was designed to sense single tone input signals, and the expected input amplitudes will not put the amplifier into saturation.

4.6 Low power operation

The minimum power consumption of the amplifier in Fig. 5 can be determined by the maximum input and output voltage swings. The minimum total current consumption of the proposed amplifier in Fig. 5 is:

$$I_{tot,min} = 2\left(\frac{V_{in,p}}{R_1}\alpha + \frac{V_{out,p}}{R_2}\beta + \gamma\right) \tag{8}$$

where α and β are current scaling factors, and γ is the total current consumption of both the current source I_2 in the transconductance stage and the output stage (Fig. 5). Equation 8 serves as a starting point to assign currents for the proposed amplifier. For example, the minimum current consumption is 266 μA, where on $\alpha = \beta = 2$, $\gamma = 0$, $R_1 = 10$ kΩ, $R_2 = 30$ kΩ, $V_{\text{in,p}} = 333$ mV, and $V_{\text{out,p}} = 1$ V. In this regard, the total current consumption can be optimized for the previously mentioned design specifications. For a given input and output swing requirement, increasing the R_1 and/or R_2 values reduces the total current consumption, but it comes at a cost of higher noise (Eq. 4) and is undesirable for a wide bandwidth amplifier. If both $I_{D2,2'}$ and $I_{D5,5'}$ are small and the input voltage is large, choosing both α and β close to 1 could put transistor $M_{2,2'}$ and $M_{5,5'}$ (Fig. 5) out of the saturation region, which degrades the THD performance. The loop bandwidth (transimpedance stage) and the output stage's slewing requirement both determine the final value of $\gamma = 130$ μA in Eq. 8. At $I_{2,2'} = 40$ μA, the pole associated at the source node of transistor $M_{3,3'}$ is above the loop gain cross over frequency. For $I_{D9,9'} = 90$ μA and a 500 fF loading capacitor at each output node, the output stage can have a THD better than −50 dB when the differential output voltage swing is 2 V_{pp} at 1 MHz.

5 Measurement results

The proposed amplifier was designed and fabricated using a 3.3 V, 180 nm CMOS process technology. Figure 11 shows the silicon microphotograph of the amplifier. The layout of the amplifier occupied 167 µm × 350 µm. The chip was assembled with a QFN package (QP-QFN100) and tested with a socket (SBT-QFN-4018) on a 4-layer PCB board.

Measured large signal magnitude response and the THD performance of the proposed amplifier is as shown in Figs. 12 and 13. The measured magnitude response of the

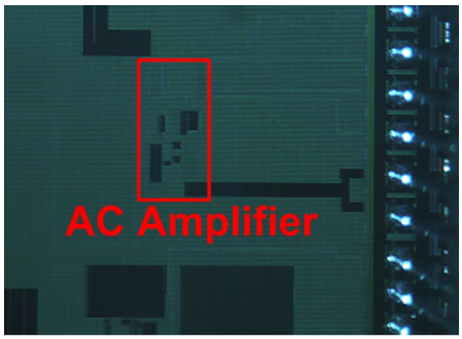

Fig. 11 A microphotograph of the fabricated chip with the proposed amplifier

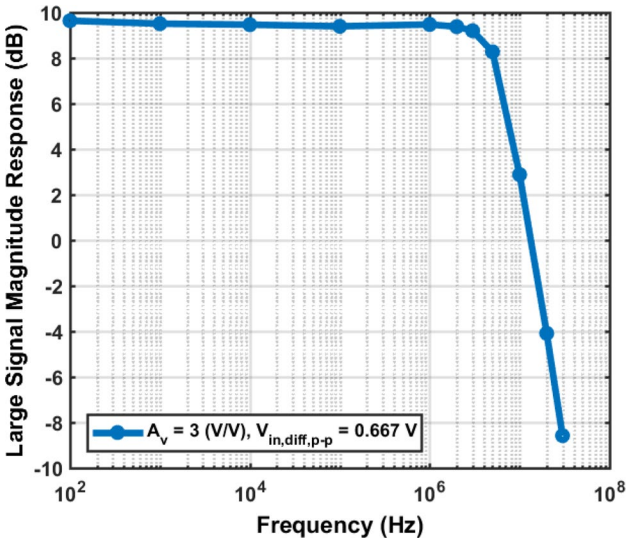

Fig. 12 Measured large signal gain versus frequency, using an input amplitude of 667 mV_{pp}

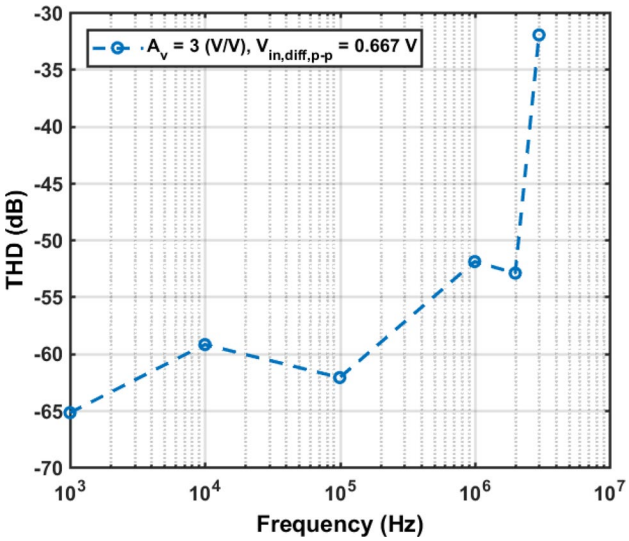

Fig. 13 Measured THD versus frequency for worst-case input amplitude of 667 mV_{pp}. Smaller input amplitudes produced lower THD

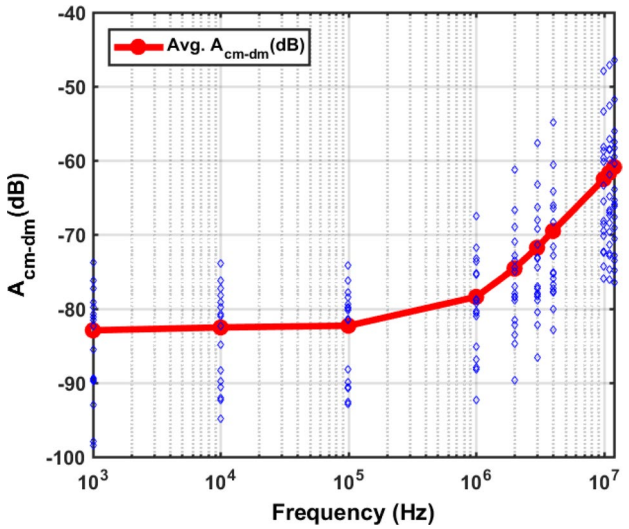

Fig. 14 Measured large signal common-mode performance of the proposed amplifier across 18 chips

proposed design is taken without a high pass filter (HPF) that is required for patient safety, to set the amplifier's input common mode voltage and to reject electrode offsets when the amplifier is used as part of the read-out channel (Fig. 1). The input differential signal was set to 667 mV_{pp} with a DC common-mode voltage of 1.39 V. As mentioned in Sect. 3, it is necessary to measure the performance of the amplifier with input voltage amplitudes above 667 mV. The measured mid-band gain of the amplifier was 9.5 dB. The variation and drift of the amplifier's gain will be accounted during the EIT system calibration [19, 31]. The measured THD in Fig. 13 includes measured harmonic content of the proposed amplifier's output, and includes the first five harmonics of the fundamental at a fixed set of frequencies. The THD performance of the amplifier is better than −50 dB up to 2 MHz.

A 1 V_{pp} sinusoidal signal, over the frequency range of 1 kHz to 10 MHz, was used to test the common-mode performance of the amplifier. This is based on the 10 mA_{pp} maximum output current of a current source regulated in the standard IEC 60601-1 [28] and assumed the contact impedance is 100 Ω [43]. The measured common-mode to differential mode gain (A_{CM-DM}) of the amplifier across 18 chips is as shown in Fig. 14. It demonstrates the amplifier has an average A_{CM-DM} close to −70 dB at 4 MHz, and an average A_{CM-DM} less than −80 dB at low frequencies. Furthermore, the amplifier was tested with input signals that have a common-mode or average input $V_{ic,pp} = (1.334 + 0.668)/2$ V = 1 V, and a differential input $V_{id,p} = 333$ mV. This mimicked the amplifier setup for the differential sensing, and

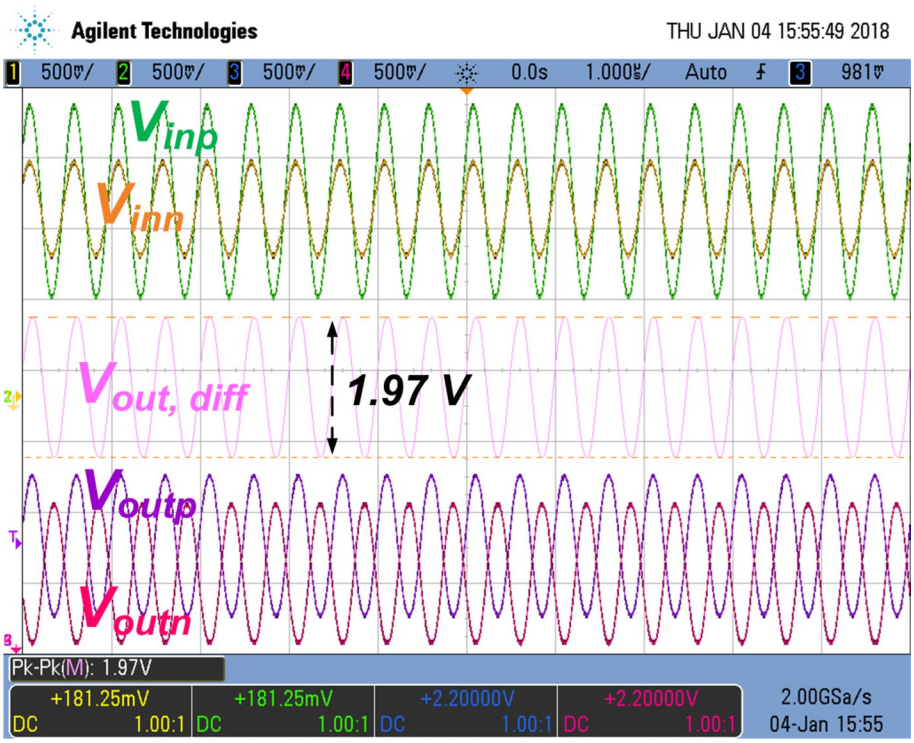

Fig. 15 Measurement results of the amplifier conditioning the input signals that have a large common-mode interference at 2 MHz

Table 1 Comparison of the measured amplifier's noise

Noise measurement in instrument	Frequency domain		Time domain	
	DSA+SA	DSA+SA	Tektronix MDO3024	Agilent MSO7014B
Bandwidth of integration	1 Hz–20.1 MHz	1 Hz –25.1 MHz	0.1 Hz –20 MHz	0.1 Hz –25 MHz
Total integrated noise (RTO)	299.82 µVrms	323.32 µVrms	310.45 µVrms	339.15 µVrms

is required to reject the common-mode interference at its input. From Fig. 12, the differential mode gain at 2 MHz is 9.19 dB. From Fig. 14, the 2 MHz common mode gain, relative to differential mode gain, is − 71.81 dB. That is, the common mode gain at 2 MHz is − 62.62 dB. The experiment depicted in Fig. 15 was done to illustrate a realistic scenario that an EIT IA faces: a large common mode signal (1 V_{pp}) occurring at the same frequency as the differential mode signal. Even in the presence of a large common mode signal, the IA still amplifies the differential signal by roughly 9 dB, as desired.

The noise performance of the amplifier was measured in both the frequency domain and the time domain. A dynamic signal analyzer (SR-785) and a spectrum analyzer (DSA815-TG) were used to capture the amplifier's output noise up to 100 MHz. In this regard, Fig. 16 shows the measured output voltage noise spectral density curve versus frequency, which follows closely with simulation result. Table 1 summarizes the measured noise performance of the proposed amplifier, and is also used to show consistency between time and frequency measurements. Each oscilloscope has

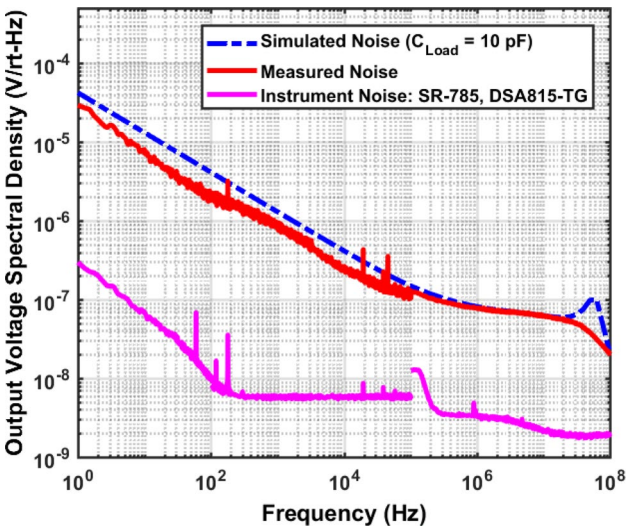

Fig. 16 Measured amplifier noise, referred to output (RTO)

a different bandwidth, total integrated noise bandwidth of frequency domain measurements were adjusted to make a better comparison. The total integrated output noise of the amplifier from Fig. 16 is 425.6 μV_{rms} (bandwidth of integration: 1 Hz –100 MHz), which is below the 1 mV_{rms} design target. The peaking at high frequency in the simulated noise spectrum (Fig. 16) is due to a high frequency zero inside the loop of the pad driver (unity gain buffer). The pad driver is used for characterizing the proposed amplifier, and its standalone noise contribution was measured and subtracted from the total measured noise to give out the amplifier's noise in Table 1.

Table 2 compares the performance of the proposed amplifier with the specifications which is part of a EIT system based on the results of the digital phantom study at Dartmouth College [6, 41], the proposed design met all the specification. Table 3 compared the measured performance of the proposed amplifier with other amplifier designs in sensor interface, biopotential acquisitions and EIT systems. To compare with other prior amplifier designs, the proposed figure of merit (FoM) based on a popular FoM in [10] can be defined as:

$$\text{FoM(dB)} = \text{SFDR(dB)} + 10 \cdot \log_{10}\left(\frac{\text{GBW}}{\text{Power}} \cdot 1\text{J}\right), \tag{9}$$

which is a normalized performance indicator employed in Table 3 to evaluate the efficiency of each design based on GBW, SFDR and power consumption. The proposed amplifier not only meets the design specification (Table. 2), but also provides the high-quality broadband signal acquisition, and shows a comparable performance (FoM) to the state-of-the-art amplifiers. In comparison with other amplifiers designed specifically for EIT applications [25, 32, 67], the proposed amplifier has the best FoM, achieves the highest SFDR and can suppress large common-mode interference at high frequencies. The noise efficiency factor (NEF) [60] is also listed in Table 3, but it only quantifies an amplifier design based on bandwidth, noise and current. Common-mode rejection and linearity, two critical performance specifications, are not included in the NEF [20].

The proposed amplifier has been successfully incorporated to build read-out channels of an EIT system [52]. We are still in the process of building and evaluating a complete 16-channel EIT system. Figures 17 and 18 are evaluation setup and preliminary result for absolute

Table 2 Summary of the amplifier's specification and measured performance

	Specification	Measured
Supply voltage	3.3 V	3.3 V
Supply current	< 1 mA	549 μA
Gain	9.54 dB	9.5 dB
Bandwidth	> 2 MHz	6 MHz
A_{CM} ($V_{in,CM}$ = 1 V_{pp})	< −72 dB	< −74 dB
THD	<−50 dB	<−50 dB
Diff. input signal range	667 mV_{pp}	667 mV_{pp}
Diff. output signal swing	2 V_{pp}	2 V_{pp}
Total voltage noise (RTO) (Bandwidth of Integration = 1 Hz–100 MHz)	< 1 mV_{rms} [a]	425.6 μV_{rms} [b]

[a] To achieve system SNR of 80 dB after a 10-bit ADC and 100 tap matched filter [42]

[b] The measured noise is higher Table 1 because the noise bandwidth of integration was 100 MHz

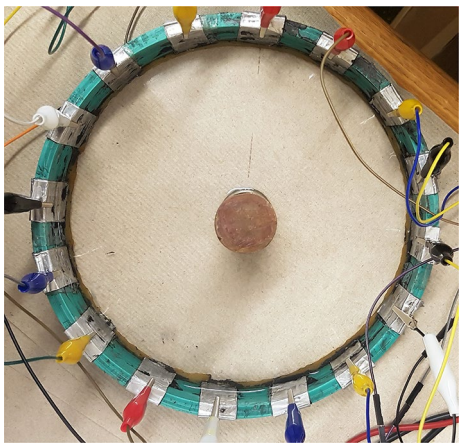

Fig. 17 A saline filled tank with 16 electrodes is developed for performance evaluation of a EIT measurement system based on the 4 channel ASICs each includes the proposed amplifier

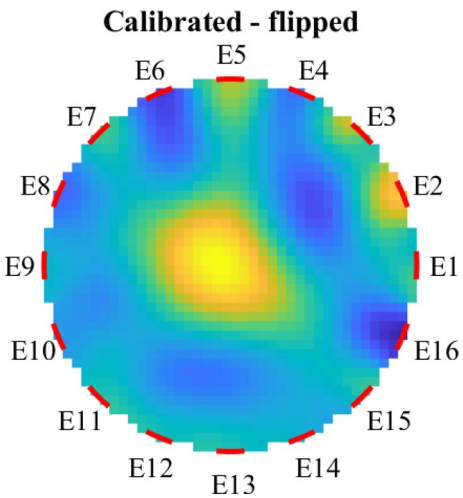

Fig. 18 Conductivity image reconstruction from the saline phantom experiment in Fig. 17

Table 3 Summary of performance comparison

	2008 JSSC [54, 71]	2011 TCAS-I [67]	2011 JSSC [70]	2011 JSSC [14]	2014 ISSCC [56]	2015 JSSC [25]	2015 ESS-CIRC [68]	2017 JSSC [32]	This work
Technology (nm)	500	350	180	65	160	180	180	65	180
Area (mm^2)	0.45	0.068	–	0.1	0.07	–	**0.02**	–	0.058
Supply Voltage (V)	3	3	1.2 – 1.5	1	1.8	1.8	1.8	**1.2**	3.3
Supply Current (A)	2.3μ	285μ	33μ	**1.8 – 2.1** μ	320μ	–	7μ	< 41μ	549μ
Diff. input range (V)	0.5m	30m	0.23m	31.48m	120m	50m	15m	50m	> **667m**
Gain (dB)	48	34	27.8	40	22.5	18	37	0/18/37	9.5
Bandwidth (Hz)	0.5 – 100	2M	20 – 280k	0.5 – 100	20k	100k	35k	1 – 300k	> **6M**
$A_{v,CM}$ (dB) $V_{inCM,pp}$ @ Freq (Hz)	−72 - @1k	−63 0.8V @2M	−63.2 -	−70 - @100	−76.5 - @30k	−72 -	−25 -	−65 - @1M	**-74** **1V @2M**
THD (dB)[a] $V_{out,pp}$ @Freq (Hz)	< −40 1.65V @ -	−56 0.5V @100k	−35.9 –	- -	−60 1.6V @21k	- -	– –	< −40 -	**-62** **2V @100k**
Noise (nV/$\sqrt{Hz}$) (RTI) (Hz)	59 0.5 - 100	9 1 - 3.14M	58 -	60 -	18.7 -	36 0.1 – 100k	40 Thermal[e]	21/45/300 Thermal[e]	**14.2** **1 – 100M**
SFDR (dB)[b]	46.3	51.2	17.8	–	**76**	–	–	40	71.7
NEF[c]	**4.3**	5.85	12.83	3.35	12.9	–	4.08	23.11	12.82
FoM (dB)[d]	141.9	161.9	128.9	–	162.7	–	–	166.8	**171.7**

Best perfomance for each specification is highlighted with bold

[a] Assumed |THD(dB)| ≈ |HD3(dB)|, and IM3(dBV) = V_{in}(dBV) - HD3(dBV)

[b] SFDR(dB) = $\frac{2}{3}$ (IIP3 - $V_{n,RTI}$), and IIP3(dB) = V_{in}(dBV) + 0.5 (V_{in}(dBV) - IM3(dBV))

[c] Only take inband noise into account

[d] $FoM(dB) = SFDR(dB) + 10 \cdot log_{10}\left(\frac{GBW}{Power} \cdot 1J\right)$.

[e] Noise density at thermal noise floor

conductivity image of experiment reconstructed from tank phantom.

6 Conclusion

The design of a broadband differential amplifier that is suitable for the EIT cardiac EIT application has been investigated. The amplifier rejects large common-mode interference at frequency of operation without tuning capacitors in a standard CMOS technology, and achieving a high FoM with respect to designs used in EIT and other sensor applications. The design meets the desired specification with a power consumption of 1.8 mW.

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Data Availability The data generated during and/or analysed during the current study are included in the article and are available from the corresponding author on reasonable request.

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