# Pathways to mm-Scale DC-DC Converters: Trends, Opportunities, and Limitations

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***Abstract*—Despite ongoing advances in semiconductor technologies, power conversion circuits and subcomponents remain a major bottleneck in a variety of performance and embedded computing applications. This paper reviews and discusses some of the fundamental tradeoffs and future prospects for high-density passive components, active devices, and circuit architectures that show promise in the direction of monolithic or mm-scale power conversion. These trends are unified in a minimum power loss figure of merit (FOM) that can be used to compare DC-DC converters under various constraints on passive components (area, energy storage, and/or volume). The paper highlights switched-capacitor and hybrid-resonant converters and outlines important trends and tradeoffs that relate to active- and passive-component utilization and conversion ratio.**

***Keywords—DC-DC converters, switched capacitor, technology scaling, resonant converters, figure of merit***

## I. Introduction

Over the past five decades, exponential semiconductor scaling has helped to revolutionize computing, communications, and information technology. For at least four of those decades, shrinking transistor sizes were used (primarily) to capture performance improvements, and expand functionality relative to size and cost [1]. However, modern technology scaling is increasingly used to address tradeoffs between *performance and power consumption* [2]. In the high-end computing space, thermal limits and *power-loss-density* have been a primary constraint on performance and a fundamental limit on clock frequency for more than a decade. This has motivated higher degrees of parallelism, the use of dynamic voltage and frequency scaling, and lower supply voltages [1]–[3]. In portable computing and a variety of embedded applications, *battery life* tends to be the fundamental limitation. There is pressure to use energy efficiently across a wide operating range and to support a number of peripheral components: wireless chipsets, displays, microprocessor(s), and sensors with an increasingly smaller volumetric footprint [4].

Unfortunately, semiconductor scaling has had a much smaller impact on power management circuits and sub-components. Efficient power electronics require passive components – inductors and capacitors – which are governed by Maxwell's equations, material properties, packaging, and practical implementation. Inductors, in particular, have remained a critical limitation to reducing size and cost. Available magnetic materials scale poorly to frequencies above 10 MHz, [5], and air-core topologies remain practically constrained to (at most) tens of nanohenries in millimeter-scale geometries, [6]. Thus it is common for power management blocks to be dominated by the size of passive components (especially inductors) and for these blocks, in turn, to dominate the board area of many communication and computing platforms. A key limiting factor is often the vertical footprint (or height) of components; many applications now require a packaged height of less than 1-2 mm.

The challenge of achieving both high efficiency and high power-density can be explored at a very high level by inspecting the well-known relationships for current and voltage ripple ($\Delta i_L$ and $\Delta v_c$) in a conventional step-down (buck) dc-dc converter:

$$\Delta i_L \propto \frac{V_{in}}{f_{sw} L}, \text{ and} \quad (1) \qquad \Delta v_c \propto \frac{\Delta i_L}{f_{sw} C}, \quad (2)$$

where $L$ is the inductance, $C$ is the capacitance, and $f_{sw}$ is the switching frequency. With a fixed input voltage, $V_{in}$, the converter requires higher inductance or higher switching frequency to reduce current ripple (or root-mean-squared current) in the powertrain. For lower voltage ripple, the converter needs higher capacitance or switching frequency.

Unfortunately, these relationships result in tradeoffs between size and efficiency. Higher switching frequencies inevitably lead to higher power loss in both active and passive components. However, if inductance is increased at a fixed volume, switching frequency may be reduced, but with the penalty of higher effective series resistance (ESR) or higher flux density (and resulting core loss), [6], [7]. With capacitors, tradeoffs present among capacitance density and breakdown voltage. For example, assuming a linear dielectric with a fixed area, capacitance scales inversely with voltage rating. Thus, trends in silicon-integrated capacitors include methods to increase dielectric surface area relative to die area – an example being deep trench surface patterning, [8]–[14].

Additional trends, and a main focus of this paper, include circuit architectures that can alleviate the tradeoffs highlighted in (1) and (2). This includes the use of hybrid switched-capacitor architectures that leverage a mixture of dielectric and magnetic energy storage, *but maximize the utility of both*. Section II will discuss passive component technologies, general scaling trends, and prospects for the future. Section III will describe active devices and how these scale with voltage rating and process technology. Section IV will outline key circuit architectures that have been presented in recent years. Section V will describe results and a comparison of topologies.

## II. Passive Components and Scaling Trends

Inductors and capacitors are the key building blocks of electronics that process, convert, and deliver energy. In any power converter that manages energy efficiently, there is a need

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to store energy, and the amount of energy storage is directly related to the eventual performance, as seen in (1) and (2). Capacitors store energy in a dielectric medium, with the governing relationship being:

$$W_d = \frac{1}{2}\varepsilon_d E_d^2 \cdot V_{ol,d}\,, \tag{3}$$

where $W_d$, $\varepsilon_d$, $E_d$, and $V_{ol,d}$ are the energy, permittivity, electric field, and volume of the dielectric respectively. Assuming a linear dielectric ($\varepsilon_d$ is constant), the maximum energy stored goes with the critical (breakdown) electric field $E_d = E_{crit}$.

Inductors store energy in magnetic field, and it can be shown that the amount of energy stored is:

$$W_m = \frac{1}{2}\mu_m H_m^2 \cdot V_{ol,m}\,, \tag{4}$$

where $W_m$, $\mu_m$, $H_m$, and $V_{ol,m}$ are the energy, permeability, magnetic field, and volume of the magnetic material respectively. Assuming a linear magnetic material ($\mu_m$ is constant), the maximum energy stored goes with the maximum (saturating) flux density $B_{sat}$, or $H_m = B_{sat}/\mu_m$.

TABLE I. COMPARISON OF ENERGY STORAGE MATERIALS

| Material | Material constant | Critical Field | Energy Density |
|---|---|---|---|
| Dielectric ($SiO_2$) | $\varepsilon_r = 3.9$ | >100 MV/m | ~300 kJ/m$^3$ |
| Magnetic (Ferrite) | $\mu_r = 1000$ | < 1 T (or ~800 A/m) | ~300 J/m$^3$ |

Table I compares two representative energy storage materials: a $SiO_2$ dielectric and ferrite magnetic material. It is seen that while the relative material constant is lower for the dielectric, the critical field is much higher. The result indicates that a $SiO_2$ dielectric can store *three orders of magnitude higher energy* per unit volume than a ferrite magnetic material. A significantly more detailed version of this comparison is presented in [15]. While there are a few caveats to this simple analysis [1], a comparison of most common magnetic and dielectric materials shows similar trends. Studies have also been conducted on commercially available capacitors and inductors, with similar conclusions, [16].

This result helps to make an argument that capacitors are potentially underutilized in DC-DC and other power conversion architectures. While inductors are the backbone of prototypical buck and boost converters, the high relative energy density of capacitors increases their favorability in size-constrained applications, [16], [17].

### A. Trends and Scaling with Capacitors

In recent years, capacitors that can be integrated in silicon processes have improved dramatically. On one hand, technology scaling has driven increasingly thin oxide layers and high-k dielectrics, which can improve capacitance density for both MOS and MIM technologies. However, oxide thinning does not directly improve energy density, which is still constrained by the electric field limit, i.e. (3). Instead, with thinner dielectrics, the compliance or breakdown voltage levels have dropped, in-line with supply voltages.

A criticism of this scaling trend is that it can be shown that with constant-field semiconductor scaling, capacitors are actually becoming relatively more expensive with shrinking process technologies. Consider the relationship for capacitance: $C \propto A/t_{ox}$, where $A$ is the area, and $t_{ox}$ is the oxide thickness. Then assuming all transistor and oxide dimensions scale by a factor, $s$ (W $\propto$ L $\propto t_{ox} \propto s$), it implies that die area scales by $\sim s^2$, whereas capacitance scales only by $\sim s$. Thus as dimensions shrink, capacitance becomes more expensive in relative terms (as a % of die area, or cost per transistor)[2], [18].

Another recent trend in integrated capacitor technology is the advancement of deep-trench capacitor fabrication. The deep-trench approach uses surface patterning of the silicon substrate to significantly increase the surface area that can be used for dielectric storage, [8]–[10]. In recent years, deep trench technologies have achieved densities of up to 500 nF/mm$^2$ [12]. These have been used successfully for monolithic switched-capacitor DC-DC converters, [19]–[22], and have helped achieve some of the highest efficiency versus power-density performance reported to date.

Fig. 1 shows trends in capacitor density over time. MOS and MIM densities are extrapolated from existing process technologies and trends in dielectrics and oxide scaling. Reported deep-trench densities are compiled from [11]–[13]. The roadmap for deep-trench capacitors is compelling as the gains in capacitance density can be in the range of 1-2 orders of magnitude higher than planar technologies.

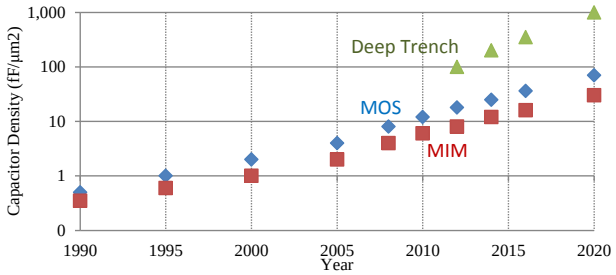


Fig. 1 Capacitor density scaling over time (compiled from [11]–[13])

In recent years, there have been foundry efforts to embed deep-trench technologies into CMOS process flows, [8], [9]. However, to date, there have been relatively few published designs that use CMOS trench capacitors for power conversion [19]–[22]. Instead, the deep-trench roadmap appears to be geared increasingly towards high-performance discrete components, [12]–[14]. While this trend is positive for discrete integration – trench capacitors may outperform ceramic capacitors in terms of linearity, stability, and loss – it is increasingly at odds with the prospect of low-cost full integration of DC-DC converters.

Going forward, circuit designers may still need to explore and exploit the capabilities of standard (low-cost) CMOS-compatible capacitors. This motivates techniques to mitigate capacitor-density limitations by operating at high frequencies, [23], [24], or to explore new architectures that can *increase utilization of available energy-density*. This latter approach is central to the value proposition of hybrid-resonant switched-capacitor converters, and will be discussed further in Section V.

[1] Constraints beyond critical field limits include current density and heat flux (thermal) limits. Pulsed-power applications, for example, can achieve very high magnetic energy density, but for a very short time duration [15].

[2] Possibly offsetting this is that scaled processes are more efficient when operating at higher frequencies; thus it may be possible to reduce capacitance requirements for the same net power loss, efficiency, or power density.

### B. Trends and Scaling with Inductors

As discussed in the introduction, magnetic components are possibly the most difficult to integrate into semiconductor processes. For example, on-chip air-core inductors are effective at RF frequencies, but less so at MHz - kHz frequencies due to scaling of quality factor, Q, with frequency. Spiral inductors are limited by the resistance of on-chip interconnect and proximity to a lossy substrate, [25]. While thick metal layers can help reduce ESR, it is still difficult to match the performance of off-chip discrete inductors. Bondwire inductors are another possibility, but are difficult to implement reliably, and still only have modest Q in the MHz range, [26].

There have also been a variety of efforts to design silicon-compatible magnetic structures that use sputtered or plated high-frequency cores [27]–[29]. Significant progress has been made in the use of thin-film magnetics and nanocrystalline materials, [28]. A variety of advanced fabrication techniques have been explored including MEMs processing and laminated sputtering, [30], and electroplating of conductors and magnetic materials, [27]. There are also efforts to develop CMOS compatible process flows for magnetic components, [29]. However, time will tell if these technologies are able to achieve sufficient manufacturing scale, low enough cost, and sufficient performance to be widely deployed in integrated power converters.

The scaling of inductor performance with size is a key factor that fundamentally limits progress in monolithic DC-DC converters. For example, capacitors can be segmented into an almost arbitrary number of small units – each retaining the same RC product or quality factor, Q. This is a key benefit of multiphase-interleaved switched-capacitor DC-DC converters, e.g. [20], [23], [24]. Inductors, on the other hand, are penalized – both in terms of efficiency and power density – by scaling to smaller size, [6], [7]. Therefore a key conclusion in [7] is that topologies that can utilize *a single magnetic component* (or core structure), have a *fundamental advantage* (smaller size and lower loss) compared to topologies that use multiple magnetic components. Also, multiphase interleaving can present a net penalty on magnetic component performance vs size, unless inductors are coupled to share a single core, as in [31].

Overall, the technology trends and scaling limitations of magnetic components will continue to present a major challenge in the pathway to mm-scale power conversion. This further motivates techniques that can improve passive-component utilization – e.g. the *volt-second/henry* relationship highlighted in (1). This consideration is also central to the hybrid-resonant SC approach and will be discussed further in Section V.

## III. Active Device Scaling Models

Active semiconductor devices have improved significantly in recent times. In silicon integrated circuits (ICs), CMOS technologies have scaled towards $f_t$ and $f_{max}$ frequencies in the near-terahertz regime [2]. This provides increasingly efficient operation at switching frequencies approaching or exceeding 100 MHz [20], [23], [32]. However, the benefits of technology scaling are correlated with decreasing supply voltages, making it more difficult to interface these technologies even with the modest voltage range of lithium batteries. At higher voltages, wide bandgap technologies have helped to relax tradeoffs among breakdown voltage, frequency, and efficiency, [33]. However, these technologies are not (yet) well suited to high-level integration, and are currently marketed mainly as discrete components.

Important figures of merit (FOMs) for active devices include size-normalized 'on' resistance, $R_{sp}$, and switching energy $E_{sp}$ [34]. The $R_{sp}$ parameter can be appreciated as the *resistance-area* product. $E_{sp}$ is the *switching energy per unit area* and can be related to specific charge, $Q_{sp}$, or capacitance, $C_{sp}$, through driving voltage levels. Thus, the power loss associated with a given device, $M_i$, can be expressed as:

$$P_{loss,i} = I_{rms,i}^2 R_{sp,i} / A_i + E_{sp,i} A_i f_{sw}, \tag{5}$$

where $A_i$ is the area of the device, $I_{rms,i}$ is the rms current, and $f_{sw}$ is the switching frequency. Importantly, $E_{sp,i}$ captures all energy loss incurred during a switching cycle that is proportional to both switching frequency and device size.

In MOS devices with low lateral electric field (typical for switching devices with low *on-state* drain-source voltage), long channel models can be used to explore scaling trends. Relationships for specific parameters can be described as:

$$R_{on} \propto \frac{t_{ox} L^2}{W L V_g}, \text{ and } E_{sw} \propto \frac{W L V_g^2}{t_{ox}}, \tag{6}$$

where $L$ is channel length, $W$ is device width, $t_{ox}$ is oxide thickness, and $V_g$ is an index of gate-drive or supply voltage. Thus, proportionality of (area) specific parameters follows as:

$$R_{sp} \propto \frac{t_{ox} L^2}{V_g}, \text{ and } E_{sp} \propto \frac{V_g^2}{t_{ox}}. \tag{7}$$

The expressions in (6)-(7) can be used to explore scaling of device parameters with process technology and/or voltage rating. Assuming constant electric field scaling and a dimensional scaling parameter, $s$, (i.e. $L \propto W \propto t_{ox} \propto V_g \propto s$), then

$$R_{sp} \propto s^2, \text{ and } E_{sp} \propto s, \tag{8}$$

or, the product $R_{sp} \times E_{sp} \propto s^3$. In the constant field scaling scenario, $s$ can also be treated as a proxy for the voltage rating of the devices, $V_r$, thus it is also true that $R_{sp} \times E_{sp} \propto V_r^3$, or that devices become worse (higher loss) at higher voltage ratings.

Another scaling regime considers a cascode arrangement of power devices. With cascoding, the voltage rating of devices remains invariant, but devices are connected in series to limit the peak electric field across any junction or oxide interface. Thus both $R_{on}$ and $E_{sw}$ scale with the number of devices in series, or

$$R_{sp} \propto s, \text{ and } E_{sp} \propto s, \tag{9}$$

and the product $R_{sp} \times E_{sp} \propto V_r^2$.

An important observation is that the scaling relationship in (9) results in the same $G \cdot V^2$ (rated conductance times blocking voltage) or, more commonly, the $V \cdot A$ (blocking voltage times rated current) cost-scaling model for active devices underlying the work by Seeman and Sanders in [17]. More importantly, it should be noted that metrics like $V \cdot A$ product are based on fundamental active-device scaling assumptions. Thus, it is important to explore *actual scaling relationships* to verify that comparisons based on these metrics will hold true.

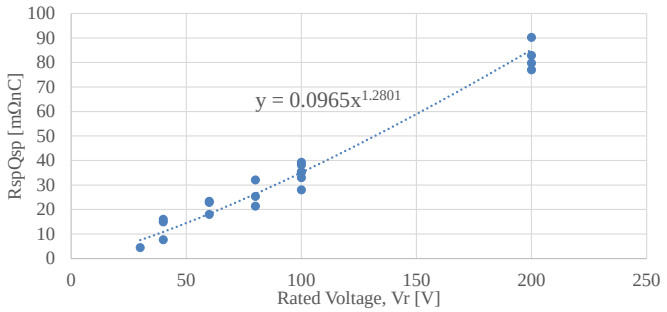


Fig. 2 Device FOM $R_{sp}{\cdot}Q_{sp}$ vs rated voltage for selected families of commercially available GaN devices, [35].

In a realistic setting, specific parameters don't always follow simple scaling laws. They depend on many different factors including *actual* electric field limits, doping, geometries, and package parasitics. Advanced technologies (e.g. superjunction mosfets and wide-bandgap devices) also scale more favorably towards higher voltage ratings. Fig. 2 shows a plot of the $R_{sp}{\times}Q_{sp}$ metric for commercially available GaN devices ($Q_{sp}$ is a proxy for $E_{sp}$ as all devices have the same gate drive voltage). A power law regression shows that $R_{sp} \times Q_{sp} \propto V_r^{1.3}$, which is better than the constant field scaling or cascode model would predict.

In [36]-[37] a more general power-law scaling model was expressed as

$$R_{sp,i}E_{sp,i} = R_{sp,0}E_{sp,0}V_{r,i}^{\alpha}, \tag{10}$$

where $R_{sp,0}$ and $E_{sp,0}$ are the specific parameters of a base-model device rated to a voltage $V_{r,0}$; $R_{sp,i}$ and $E_{sp,i}$ are the specific parameters of a device rated to voltage $V_{r,i}$ which is normalized to $V_{r,0}$; power law parameter, $\alpha$, captures the scaling trend.

## IV. DC-DC Comparison Framework

The scaling relationships in the previous section can be used to derive a figure of merit (FOM) for comparing arbitrary DC-DC converter topologies. A full derivation and discussion of this FOM is presented in [36], [37], and thus it is presented in condensed form here.

Consider first the relationship shown in (5), which describes power loss in an arbitrary switching device, $M_i$, which is loaded with current, $I_{rms,i}$, and operates at frequency, $f_{sw}$. Assuming the area (or width) of the transistor is adjusted arbitrarily to minimize the sum of conduction and switching losses, the minimum power loss follows as:

$$P_{\min,i} = 2I_{rms,i}\sqrt{f_{sw}}\sqrt{R_{sp,i}E_{sp,i}}\ . \tag{11}$$

This expression can be expanded by summing over all switching devices, in the converter to give

$$P_{total} = 2\sqrt{f_{sw}}\sum_{i\in switches} I_{rms,i}\sqrt{R_{sp,i}E_{sp,i}}\ . \tag{12}$$

where $P_{total}$ is the total (minimum) power loss in the active devices in the converter.

This can be reformulated into a charge-multiplier treatment by using a notation similar to the one used in [17]. Here, the charge multiplier is defined as the ratio of average (dc) current in the switch to the total output current of the converter:

$$a_{r,i} = I_{dc,i} / I_{out}\ . \tag{13}$$

To accurately capture loss, a term $\beta_{r,i}$, which is the ratio of rms/dc current in the switch is used to set up the following relationship:

$$I_{rms,i} = \beta_{r,i}a_{r,i}I_{out}\ . \tag{14}$$

The relationships in (11) and (14) can then be combined with the scaling relationship for specific parameters in (10) to give the following expression for minimum power loss of the converter:

$$P_{total} = 2I_{out}\sqrt{R_{sp,0}E_{sp,0}}\cdot\sqrt{f_{sw}}\sum_{i\in switches}\beta_{r,i}a_{r,i}V_{r,i}^{\alpha/2}\ . \tag{15}$$

Importantly, it may be noted that $R_{sp,0}$ and $E_{sp,0}$, and $\alpha$ are representative specific parameters for a given process technology. Thus, in (15), the switching frequency, and $\Sigma\beta_{r,i}a_{r,i}V_{r,i}$ term are dependent on the converter topology. As discussed in [36], [37], the topology-dependent portion can be used as a FOM for arbitrary DC-DC converter topologies:

$$FOM = \sqrt{f_{sw}^{*}}\sum_{i\in switches}\beta_{r,i}a_{r,i}V_{r,i}^{\alpha/2}\ . \tag{16}$$

The figure of merit (16) can be thought of as a normalized performance limit for *minimum achievable power loss*, thus *a lower value is better*. Parameter $f_{sw}^{*}$ represents the normalized effective switching frequency; the '*' indicates that (16) is only meaningful if a uniform constraint for $f_{sw}$ can be developed.

In [36], [37], constraints were applied to the passive components, for example: total area, volume, or peak energy storage of capacitors and inductor(s). In this case, the metric, $f_{sw}^{*}$ is representative of *passive component utilization*: a converter that uses passive components more effectively will operate at a lower frequency. On the other hand, the $\sum\beta_{r,i}a_{r,i}V_{r,i}^{\alpha/2}$ expression is representative of *active device utilization*. For example, with $\alpha = 2$ and $\beta_{r,i} = 1$, this breaks down to the familiar sum(VA) term used commonly for a device utilization metric. The $\beta_{r,i}$ term is then a correction factor that considers the actual rms currents that flow in the semiconductor switches.

In principle, the FOM in (16) can be used to explore or compare performance for any DC-DC converter, provided a suitable constraint can be constructed for $f_{sw}^{*}$. For resonant or hybrid-class switched capacitor converters, which we will explore next, we will use the resonant frequency as the constraint. Voltage ripple at the input or output terminal might be another suitable constraint, given some allocation of bypass capacitance. Another strategy might be to hold $f_{sw}^{*}$ constant, and explore the ramifications (across converters) on the $\Sigma\beta_{r,i}a_{r,i}V_{r,i}$ expression.

## V. Circuit Architectures

Over the past decade, a number of circuit architectures have been explored in an effort to relax the efficiency versus power-density tradeoffs of conventional buck or boost converters. Switched capacitor (SC) DC-DC converters have been studied extensively due to their favorable utilization of both active and passive components, [16], [17], and because they benefit more directly from the relatively high energy-density of capacitors, as discussed in Section II.

SC converters have a number of very favorable characteristics. Because capacitors can be segmented into an almost arbitrary number of parallel units without degrading the quality factor of each, high-order multiphase interleaving is an attractive

option, [23]. Interleaving helps to increase capacitance utilization as input and output voltage ripple can be reduced (almost) arbitrarily, eliminating the need for bypass capacitance [20]. A number of exciting techniques have been developed to eliminate (previously) problematic issues such as *bottom-plate switching loss* in multiphase interleaved designs [38].

However, notable challenges with the SC approach include achieving variable voltage regulation without sacrificing efficiency or power-density. While the first-order dynamics of SC converters combined with high switching frequency have enabled fast transient response, [21], [39], regulation is still challenging as it requires some form of linear regulation and/or reconfigurable (gear-box) approach [21], [23], [40]. Due to the added complexity and additional parasitics of gear-box capable converters, power-density has been observed to be falling with an increasing number of gear-box conversion ratios [41].

The tradeoffs between efficiency and power density are also somewhat rigid with SC converters. These typically include higher charge-sharing losses at lower switching frequencies (in the *slow-switching limit*, SSL), and higher frequency-dependent losses at higher frequencies (in the *fast-switching limit*, FSL). Aside from better process technologies (deep-submicron and silicon on insulator, SOI), and higher capacitance density (e.g. deep trench) there have been relatively few techniques proposed that can address or mitigate these tradeoffs, [42].

Hybrid and resonant switched capacitors provide one path forward to alleviate tradeoffs between frequency-dependent and conduction losses. In hybrid-resonant converters, a native SC stage is augmented with one or more inductive impedance(s). The inductor is used to 'shape' the current waveform in a manner that reduces or eliminates charge-sharing ($CV^2$) loss. In resonant operation, the voltage swing on flying capacitors is increased by ~Q (the quality factor of the resonant circuit). This *improves energy-density utilization* of capacitors by ~$Q^2$, [36]. On the other hand, the inductor may be much smaller (10-100×) than in a buck or boost converter because the SC stage reduces the voltage across the inductor, i.e. [V·s/H] relationship in (1).

Fig. 3 shows a generic hybrid-SC converter where a single inductive impedance is lumped at the output terminal. This approach has been used for SC topologies where all charge-flow links the output terminal, and thus the converter can be soft-charged with a single inductor, [36], [45]. Perspectives on a broader multi-mode suite of operating modes have been discussed in [46]–[50], and are highlighted in Fig. 4. The multi-mode perspective outlines a range of different (soft-charging) current waveforms possible for hybridized SC converters.

Going back many years, there have been proposals to augment conventional DC-DC topologies with SC stages or multiplier cells, [43]. Middlebrook, for example, proposed hybridizing the Cuk converter with (what is effectively) a series-parallel SC converter almost 30 years ago, [44].

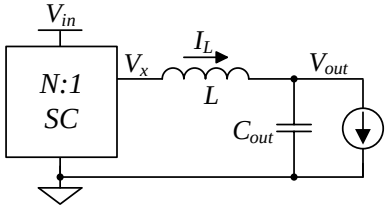


Fig. 3 Generalized hybrid SC converter, [36], [45].

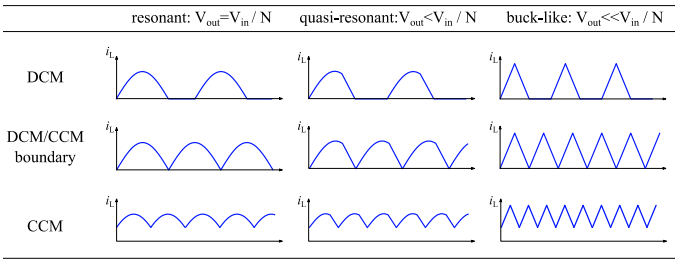


Fig. 4 Hybrid-SC multimode inductor current waveforms, [36], [46], [47].

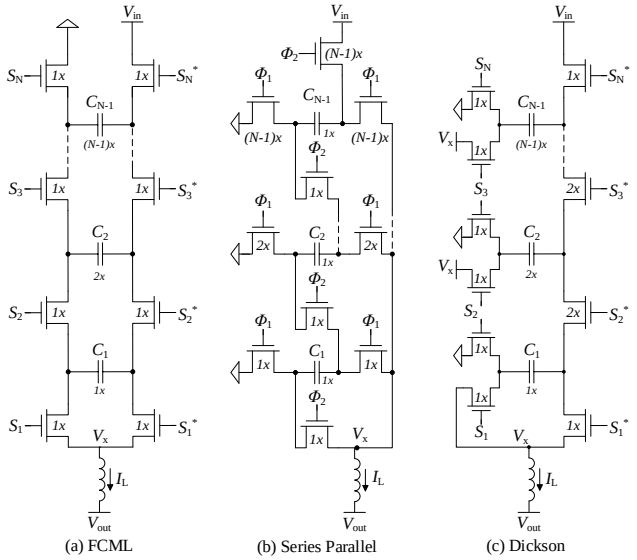


Fig. 5 Common SC topologies hybridized with an inductive impedance, [37].

In most of the work that can be classified as hybrid SC, the treatment of the inductor current waveform is as a traditional ramp waveform. A common example is the Meynard, or flying-capacitor multilevel (FCML) topology Fig. 5(a), which is most commonly treated as a multilevel buck converter [51], [52]. However, as shown in Fig. 3, many other operating modes are possible. Resonant operation may be achieved for nominally unregulated operation when the output voltage is the same as the native (unregulated) SC conversion ratio, *N*. Quasiresonant operation can be used to implement modest regulation around a nominal resonant operating point, [48], [49]. And finally, inductive (buck or boost) operation may be used to achieve more aggressive regulation away from the nominal SC conversion ratio [46], [52], and where the switching frequency is much higher than the resonant frequency of the LC network.

Additional operating modes include distinctions such as continuous or discontinuous conduction. For example, at high load, the switching frequency can be increased to affect continuous current conduction (CCM) and reduce the rms/dc current in the inductor. At light load, a dead-time or 'off-time' can be introduced, affecting discontinuous conduction (DCM) operation and providing a linear tradeoff between switching and conduction loss, [50]. Similar modes are possible with resonant, quasiresonant, and inductive current waveforms, [46], [47].

Importantly, the qualifying distinction of a '*resonant switched capacitor*' (ReSC) converter is related to the *operating mode – not the circuit architecture*. Historically, ReSC converters have operated with a sinusoidal inductor current trajectory and zero-current switching (at the DCM boundary), [53]–[55]. However, a multitude of other operating modes are available to converters that hybridize a SC stage with an inductive impedance.

## VI. Topology Comparison

There are many possible SC topologies that are amenable to hybridization with an inductive impedance. Fig. 5 highlights several of the most common architectures, but others include Fibonacci, ladder, the recently proposed 'stacked-ladder' converter, [56], and others, [57]. In [17], a framework was developed to compare SC topologies relative to their merits in passive and active component utilization. More recently, the framework in Section IV has been used to compare hybrid topologies operating in the resonant mode [36], [37].

TABLE II. General Merits & Comparison: Hybrid-SC Topologies

| Topology | Notes |
|---|---|
| FCML | • Intermediate active-device utilization, all single-voltage rated devices<br>• Intermediate passive-component utilization; moderate to low normalized switching frequency<br>• Straightforward multilevel operation; multiplication of effective switching frequency |
| Series-Parallel | • Worst active-device utilization, high voltage rated switching devices<br>• Best passive-component utilization, lowest normalized switching frequency |
| Dickson | • Best active-device utilization<br>• Worst passive-component utilization, highest normalized switching frequency<br>• Conventional Dickson topologies require a 'split-phase' control scheme to prevent internal charge sharing, [58] |
| Fibonacci | • Intermediate in both active and passive utilization<br>• Highest conversion ratio per number of switching stages or capacitors |
| Stacked Ladder | • Similar to Dickson, but does not require split-phase operation<br>• Requires at least 2-phase interleaving to eliminate bypass capacitors at intermediate stages |

Overall, SC, [17], and ReSC, [37], analyses identify similar relative merits of the different topologies. Table II highlights general features and a relative comparison of topologies. For example, Dickson-based topologies are found to have the best active device utilization, while series-parallel has the best passive component utilization. Flying capacitor multilevel (FCML) converters are intermediate in both active and passive utilization, but have a straightforward implementation and are capable of multilevel operation. The 'stacked-ladder' topology, [56], can be appreciated as a version of the Dickson that uses 2-phase interleaving to eliminate both internal charge sharing loss, and the need for intermediate bypass capacitors.

The singular figure of merit (FOM) in (16) can provide a more quantifiable comparison of the different topologies. In [37] this was used to explore relative performance (minimum loss) versus conversion ratio of different topologies. A uniform comparison was completed by constraining the *total area or energy storage (a proxy for total volume) of flying capacitors*. The total area or volume is allocated according to the number of flying capacitors while considering their relative voltage rating. Several different loss models were also considered for the inductor(s).

Table III summarizes the results of this study by highlighting the best (minimum achievable power loss) converter at a given conversion ratio, $N = V_{out}/V_{in}$. In a scenario where there is *no loss penalty for increasing inductance*, it is found that Dickson-based topologies outperform others, especially at higher conversion ratios. The advantages of Dickson topologies (including the stacked-ladder) result from their high active-device utilization: as conversion ratios increase, Dickson topologies use switches more effectively and thus have lower net resistive losses (higher conductance) per unit of blocking voltage.

At lower conversion ratios, passive component utilization becomes more important. With a *lossless inductor*, FCML is slightly better with area-constrained capacitors; series parallel (SP) is slightly better with volume-constrained capacitors. SP topologies, in which all flying capacitors are rated to the same (low) voltage, tend to perform better with the volume or energy constraint because this penalizes high-voltage-rated capacitors more than the area constraint. FCML, which requires (some) high-voltage capacitors, tends to perform better in the area-constraint which has a less strict penalty on voltage rating.

TABLE III. Summary of Topology Comparison from [37]

| Inductor Model ↓ / Capacitor constraint → | Total Area (flying capacitors) | Total Energy or Volume (flying capacitors) |
|---|---|---|
| Lossless inductor | • Dickson @ N > 3<br>• FCML @ N < 3 | • Dickson @ N > 3<br>• SP @ N < 3 |
| DC resistance dominates loss | • Dickson @ N > 5<br>• FCML @ N < 5 | • Dickson @ N > 6<br>• SP @ N < 6 |
| AC (skin effect) loss dominates | • Dickson @ N > 6<br>• FCML @ N < 6 | • SP best, all conversion ratios |
| AC (prox. or core) loss dominates | • Either SP or FCML | • SP best, all conversion ratios |

In a scenario where DC *(frequency-invariant) resistance* dominates loss in the inductor, Dickson-based topologies are still best at high conversion ratios, but the crossover or inflection where FCML and SP outperform increases to a conversion ratio of N ~5 and N ~6 respectively for area and energy constrained capacitance. This is a reflection that *passive component utilization becomes more important when inductor losses are factored in*. In a scenario where AC *(frequency-dependent) resistanc*e dominates loss in the inductor, the advantages of FCML and (particularly) SP topologies increase. This is again related to passive component utilization. For example, it can be shown that with a given inductance and capacitance allocation, the series-parallel topology is capable of switching at the lowest frequency of all known topologies, [37].

The high passive-component utilization of the series-parallel topology results in an important observation. In scenarios that penalize high frequency operation: skin effect (inductor $ESR \propto \sim f_{sw}^{½}$), core loss ($\propto \sim f_{sw}^{1.5}$), and proximity effect ($ESR \propto \sim f_{sw}^{2}$), the relative benefits of the series-parallel topology tend to increase. Active-device utilization and its relationship with the power-law scaling parameter, $\alpha$, in (10) also has an important impact. With high $\alpha$, Dickson topologies benefit, but with low $\alpha$ (e.g. GaN, SiC or superjunction devices) series-parallel topologies are increasingly favorable.

While there are a number of other factors that need to be considered (e.g. bottom-plate switching losses, resistive losses in interconnect and capacitors, complexity of gate driving, and control), the results highlight that passive component utilization is a key factor in selecting a converter topology. Thus, *conventional converter metrics such as V·A product provide only part of the picture when both efficiency and size are important*. Also, topologies like series-parallel, which have received only limited attention in the hybrid-SC literature, may prove to be among the best candidates for high-density dc-dc converters due to their better utilization of passive components.

## VII. Design Example and Considerations

Here we provide a brief example of a hybrid series-parallel SC converter, originally presented in [41], [59]. In this work, the series-parallel topology was modified to operate with all single voltage rated n-channel transistors. It used a quasiresonant operating mode, i.e. Fig. 4, to provide variable regulation (12V:3.7V) and 1-bit voltage-mode integral control with nested zero-current regulation. A photo of the implementation is shown in Fig. 6. The converter used small (0402 and 0201) off-chip flying and bypass capacitors, and an 0402 36 nH inductor. Measured efficiency was 87.5% at an output power of 4.6 W, and total solution area (bounding box of PCB area) of ~20 $mm^2$ and solution height < 1 mm (including PCB).

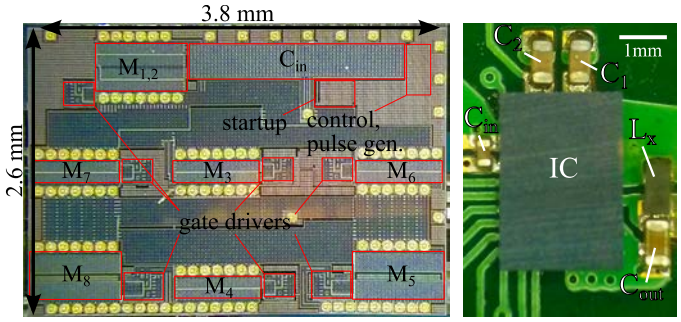


Fig. 6 mm-scale series-parallel converter 87.5% efficiency @ 4.6W from [59].

Key considerations and design novelties in [59] included a zero-current detection (ZCD) scheme to regulate the valley currents in the inductor waveform. The ZCD scheme was also used to affect zero-voltage switching on the low-high switching transitions. To ensure safe startup, the design used a pre-charge circuit to initialize voltages on the flying and bypass capacitors. The gate drive scheme used bootstrapping from various fixed and flying nodes to drive the n-channel power devices. Finally, a careful design and layout was used to reduce parasitic inductance and ringing on the switching node. While the control scheme could have been improved to have faster transient response, this was a promising first demonstration of a mm-scale, hybrid switched-capacitor series-parallel converter.

## VIII. Conclusion

There is a growing need for small and efficient power management circuits and subcomponents in a variety of applications. While capacitors and inductors have improved in recent years, there is still a need to explore circuit architectures that maximally leverage their power- and energy-density. Switched-capacitor DC-DC converters are promising, but are still limited by fundamental tradeoffs among efficiency, power-density, and voltage regulation capabilities. Hybrid-class SC converters can alleviate some of these tradeoffs by reintroducing small magnetic components. A framework to compare different architectures was presented using a minimum power loss figure of merit. Architectures that have better active-device utilization tend to be more favorable at high conversion ratios; those with better passive component utilization tend to outperform at lower conversion ratios. However, when frequency-dependent losses in magnetic components are factored in, and with process technologies that scale better to high voltage, topologies like series-parallel (SP) and flying-capacitor multilevel (FCML) seem attractive for a variety of future applications.

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