A Highly-Integrated Series-Parallel Switched-Capacitor Converter with 12-Volt-Input and Quasi-Resonant Voltage-Mode Regulation

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***Abstract*—This work presents an integrated circuit (IC) implementation of a hybrid switched capacitor converter based on a modified series-parallel architecture. The converter operates in a quasi-resonant mode to regulate a nominal 3.7 V output from a 12 V supply. The design uses zero-current detection and nested 1-bit regulation to autotune the zero-current switching state, simplify the design of a digital voltage-mode control scheme, and achieve partial zero-voltage switching (ZVS). The modified architecture is able to operate with single-voltage rated devices without degrading the VA product of the converter. The paper discusses details of level shifting, gate driving, and bootstrapping for an all n-channel powertrain, including a precharge circuit to facilitate safe startup. The converter IC was designed in 180 nm bulk CMOS with a 5 V option for power devices. It was tested in a flipchip assembly with a 36 nH 0402 inductor to deliver up to 4.6 W at 87.5 % efficiency at a power density of 0.23 W/mm3.**

***Index Terms*—DC-DC converter, switched capacitor, resonant switched capacitor, integrated circuits**

I. INTRODUCTION

In modern power electronics, there is a constant need to improve efficiency to extend battery life of portable electronics, relax thermal constraints in high-power applications, and help mitigate carbon emissions by reducing wasted energy. However, in a variety of applications, *form-factor, area, volume, and ultimately the power-density of energy-management components are becoming critical* as these constrain both size and cost of the packaged system [1]–[3]. The most common power delivery architectures are heavily dependent on magnetic energy storage. In recent times, buck, boost, and transformer-coupled DC-DC converters have dominated the market for applications at low-moderate voltage and power levels. This has placed significant pressure on inductive components to operate with increasing volumetric power- and energy-density and low loss at higher switching frequencies [3].

This challenge can be illustrated by considering the well-known relationships for voltage and current ripple (Δv_c and Δi_L) in a conventional step-down (buck) DC-DC converter:

$$\Delta i_L \propto \frac{V_{in}}{f_{sw} L}, \text{ and} \quad (1) \qquad \Delta v_C \propto \frac{\Delta i_L}{f_{sw} C}. \quad (2)$$

Here, L and C are the respective inductance and capacitance, V_{in} is the supply voltage, and f_{sw} is the switching frequency. The units of (1) are [V-s/H] and units of (2) are [A-s/F]. These relationships demonstrate clear tradeoffs among switching frequency, input voltage, and passive component size. For example, to improve the [A-s/F] FOM for a fixed Δi_L, higher frequency or larger capacitance is needed. Similarly, improving the [V-s/H] FOM requires increasing either frequency or inductance. Therefore, in future applications, achieving higher power-density will necessitate either: a) higher operating frequencies and an inherent tradeoff with efficiency, or b) efforts to rethink or restructure the most common power electronic architectures to circumvent or alleviate these tradeoffs [3]–[6].

Fortunately, active devices trends generally support operation at higher switching frequencies. In silicon integrated circuits, CMOS technologies have scaled towards f_{max} levels in the near-THz regime [7]. This provides increasingly efficient operation at switching frequencies approaching or exceeding 100 Mhz, [8]–[10], although notably with devices rated to 1 V or less. At higher voltages, wide-bandgap technologies have helped to relax tradeoffs among breakdown voltage, frequency, and efficiency, and are trending towards higher levels of integration [11]. Capacitor technologies are also improving, one example being deep-trench technologies with densities approaching many 100s of nF/mm^2 – orders of magnitude higher than traditional MIM and MOS capacitors [12], [13]. However, magnetic components remain a key limitation. Available magnetic materials scale poorly to frequencies above 10 MHz, and air-core topologies remain practically constrained to (at most) tens of nH for mm-scale geometries [14].

Hybrid, resonant, and soft-charging operation of switched capacitor (SC) converters is increasingly promising to address some of the above-mentioned limitations [15]–[18]. The hybrid approach leverages the advantages of SC converters, namely the relatively high energy-density of capacitor components, [2],

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favorable utilization of active-devices, [4], and scalability in silicon integrated circuit technologies, [19]. In general, SC approaches are effective at achieving large, nominally unregulated voltage conversion ratios. However, the hybrid approach uses a small inductor to shape the current waveform that flows in the SC stage. From the perspective of the SC converter, the additional magnetic component helps to reduce or eliminate charge-sharing losses, increasing utilization of the energy-density of the flying capacitors. It also provides an efficient means to perform variable regulation of the output voltage without gear-box or linear regulation methods [20], [21].

From the perspective of traditional inductor-based DC-DC converters, the SC stage can significantly reduce the V/H quantity in (1), enabling the use of a much lower switching frequency or smaller inductor. In practice this can reduce the needed inductance (or inductor volume) by factors as high as 10-100x, in some cases allowing the use of nano-henry regime air-core inductors [20].

While, in theory, all SC topologies can be augmented with additional magnetic components. Only a subset of the most common topologies can be resonated or soft-charged with a single inductor. The use of a single inductor coupled to either the input or output terminal can be perceived as an advantage as it represents only a modest increase in bill of materials, cost, and complexity. The analysis in [15] can be used to identify several prime candidates including Dickson, Fibonacci, series-parallel, and flying capacitor multilevel (FCML) converters. The work in [22] compared these topologies, as well as the recently proposed 'stacked-ladder' converter, [23], in terms of 'minimum achievable power loss' when subject to a common (area, volume, or energy storage) constraint on passive components. While Dickson-based topologies achieve the best active device utilization figure of merit (lowest conduction loss for a fixed voltage times current (VA) rated design), they are among the worst in terms of passive component utilization. The series-parallel topology, on the other hand, is poor in its use of active devices (VA rating), but has the best utilization of capacitors. Overall, it was found in [22] that when given strict size constraints to passive components, and when factoring in (particularly frequency dependent) losses in the magnetic components, the series-parallel was one of the best for moderate conversion ratios (below ~6:1). While the series-parallel topology has received a great deal of attention in the SC literature, its potential as a hybrid-class converter has gained noticeably less attention.

In this work, we explore the series parallel converter and its prospects for operation with a single soft-charging inductor. We develop a modified series-parallel architecture that can be implemented with all low-voltage rated switches without affecting the overall converter VA rating. An experimental integrated circuit (IC) prototype highlights a nominally 3:1 resonant switched-capacitor (ReSC) converter that merges a series-parallel SC front end and a mm-scale, 36 nH off-chip inductor. The design implements closed-loop variable voltage regulation, interfacing from a nominal 12 V supply to a 3.5-4 V output. Variable regulation is achieved through quasi-resonant operation that includes partial resonant transitions and hard-switched (buck-like) switching states. Closed loop control is achieved by using a sampled hysteretic comparator and 1-bit digital integral control. A zero-current detection scheme is used to ensure quasi-resonant operation and self-tuned zero-current switching.

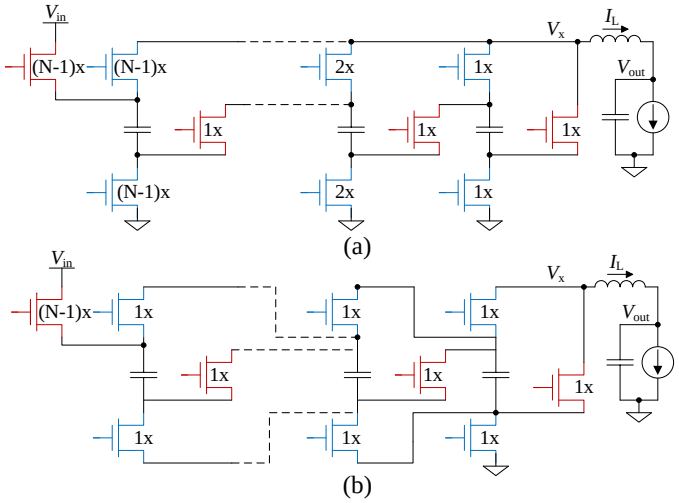


Fig. 1 Comparison of a.) conventional SP topology and b.) modified SP topology.

II. TOPOLOGY OVERVIEW

Fig. 1(a) shows a schematic representation of a conventional *N:1* series parallel topology, where *N* is the nominal, unregulated step-down voltage ratio ($N = V_{in}/V_{out}$). The series-parallel converter consists of *3N-2* switches, and *N-1* flying capacitors, with each capacitor rated at V_{out} (here, *1x* will represent a voltage rating equal to the output voltage). A total of *N-1* switching pairs are used to configure the capacitors in the parallel phase (shown in blue). These are rated to increasing voltage in integer increments from 1x to (*N-1*)x working from the output to input terminal. An additional *N* switches are used to configure the capacitors in the series phase (shown in red). These are all rated to *1x* the output voltage, with the exception of the final switch that connects to the input terminal, V_{in}. As the charge multiplier component for all switches is $A_{r,i} = 1/N$, the VA product for the converters is computed by summing the voltage rating over all switches, $V_{r,i}$, divided by the nominal conversion ratio, *N*. This procedure gives:

$$\sum_{i \in switches} V_{r,i} A_{r,i} = \frac{(N+1)(N-2)}{N}. \qquad (3)$$

A modified circuit that implements the same SP function is shown in Fig. 1(b). Here, each of the successive parallel-state switches are configured in series. Because, in the series phase, each of these switches is now only exposed to the voltage across one of the flying capacitors, they are rated at only *1x* the output voltage. However, because the parallel-state switches are connected in series, their charge multiplier component increases in integer increments, i.e. $A_r = 1x, 2x, \ldots, (N-1)x$, for switches closer to the output terminal. Therefore, when the VA sum is computed, the result is the same as in (3). However, the

final switch that is coupled to V_{in} remains with both the same voltage rating and charge multiplier. Therefore, while the majority of switches can be implemented with a single voltage rating, the input-coupled switch must still block a large fraction of the input voltage. As will be discussed in the next Section, this final switch may be configured with cascoded devices to achieve an all single-voltage rated design.

III. NOMINAL 3:1 TOPOLOGY AND CONTROL SCHEME

In this work, the goal was to target an efficient interface between 12 V and 3.7 V bus domains. Operation from a 12 V bus is relatively standard in both performance computing and automotive applications (or, more broadly, applications supported by lead-acid batteries). The 3.7 V bus potential is increasingly common for portable computing and other applications supported by lithium-ion technologies. Therefore DC-DC converters that can efficiently move power between these domains are gaining importance. The conversion ratio of 12:3.7 is well suited for a nominally 3:1 converter architecture as this is slightly below the nominal (unregulated) output of 4 V. The modified series parallel topology, shown in Fig. 2, was used for this purpose. To achieve efficient operation with a 12 V input, the converter in Fig. 2 used switches rated for 5 V, which provided some margin of safety given the nominal output of 4 V, and regulated voltage levels between 3.5-3.8 V.

The converter in Fig. 2 uses the modified scheme discussed in Section II to ensure the *1x* rating for devices M_3-M_8. The input-coupled switch uses a *1x* rated cascode (M_1), and a *1x* rated switching device (M_2) in order to use all 5 V rated devices. It can again be found that this circuit achieves the same VA rating as the conventional design. However, all devices, except for M_5, are now referenced to floating nodes which complicates the gate-drive circuitry. Although the modified topology introduces some additional complexity, it enables implementation in a standard CMOS process with just one type of transistor.

Similar to what was shown in [21] for a 2:1 SC converter, the series-parallel topology can be operated in nominal resonant operation as well as a 'quasi-resonant' or 'buck' operating mode. The three circuit states are shown in Fig. 3 for the modified series-parallel topology. In the 'series' state, $M_{1\text{-}4}$ are switched *'on'* and connect the two flying capacitors in series between V_{in} and the switching node. During the 'parallel' state, $M_{5\text{-}8}$ are turned on and connect the two flying capacitors in parallel between the switching node, V_x, and ground. Another state, termed 'buck' state, is introduced to achieve variable conversion ratio operation. In the 'buck' state, the switching node is connected to ground through M_4 and M_5, while the capacitors are disconnected.

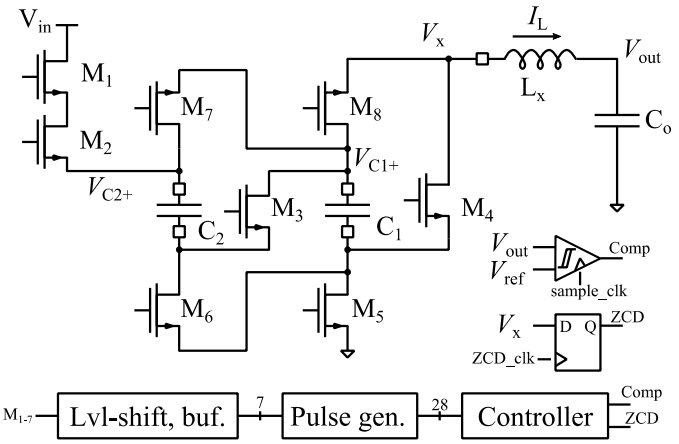


Fig. 2 Modified 3:1 SP converter and key circuit blocks

In resonant operation, the circuit alternates between the 'series' and 'parallel' state. During each state, a resonant half-cycle is completed, however, the time spent in the parallel state is longer as the time spent in the series state. This follows from the resonant period of the LC network which is proportional to the square root of the product of L_x and C^*, where C^* is the effective capacitance seen by the inductor in a given state. For the generic *N:1* series parallel topology (i.e. Fig. 1) with total flying capacitance, $C_T = (N\text{-}1)C_x$, in the parallel phase $C^* = C_T$, while in the series phase $C^* = C_T/(N\text{-}1)^2$. Therefore, the effective switching frequency, f_0^*, of the arbitrary converter in resonant operation follows as:

$$f_0^* = \frac{N-1}{N}\frac{1}{\pi\sqrt{L_x C_T}}. \tag{4}$$

An important observation can be made from the relationship in (4). For higher conversion ratios, *N*, the switching frequency will increase, largely because the time duration of the series state is reduced with more of the total capacitance in series. However, compared to a nominal 2:1 converter with the same total capacitance, C_T, the switching frequency, $f_0^*(N)$, asymptotically approaches $2 \cdot f_0^*(N=2)$, or a maximum increase of 2x relative to the nominal 2:1 converter. This is a nice feature of the SP topology, and is related to the capacitance-utilization figure of merit derived in [22]. In effect, for a given total capacitance allocation (or total dielectric energy storage), *the SP converter is capable of resonating at the lowest switching frequency of any SC topology*. This benefit is quantified in terms of power loss and efficiency, as a lower switching frequency can help offset the poor active device figure of merit (or VA) product compared to topologies such as the Dickson. For reference, in the 3:1 topology in Fig. 1, the time duration of the parallel phase is twice as long as the series phase. The effective switching frequency in resonant operation is:

$$f_0^* = \frac{4}{3}\frac{1}{2\pi\sqrt{L_x C_T}}, \text{ for } N = 3, \tag{5}$$

or 4/3 the switching frequency of a 2:1 design with the same total capacitance.

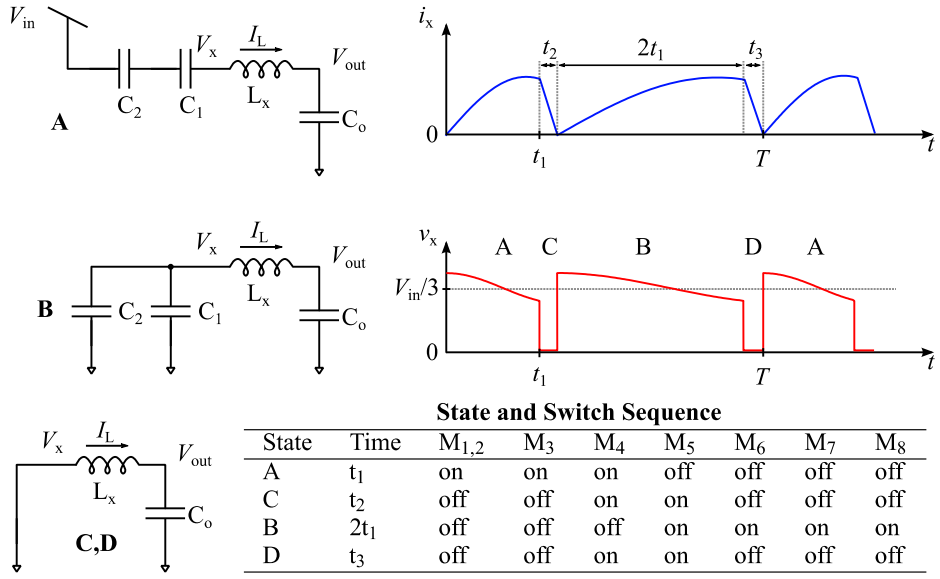
IV. IMPLEMENTATION DETAILS

A. Quasi-resonant feedback control

Fig. 3 shows the basic operation of the converter with the timing and switch configuration in each operating state. In state-A the capacitors are configured in series between the input and the switching node for a time period of t_1. The current waveform follows a partial resonant cycle with nominal resonant period defined by the inductance, L_x, and series combination of C_1, C_2, and C_0. During state-C the switching node is connected to ground for a period of t_2 until the current reaches zero (determined by zero-current detection). In state-C the flying capacitors are configured in parallel between the switching node and ground for a period of $2{\cdot}t_1$, followed by state-D during which the switching node is again connected to ground for t_3 until the current reaches zero. By using t_1 as the control variable and autotuning t_2 and t_3 to achieve zero-current switching, the converter can be operated in feedback to regulate the output voltage.

Active zero-current detection, shown in Fig. 4, is critical to this operating sequence. Here, zero current detection (ZCD) is achieved by sampling the switching node voltage at the end of the deadtime interval following states C and D, synchronous with the 'turn on' gate signal for M_5 and M_4 respectively. A similar scheme was used for buck converters operating in discontinuous-conduction mode (DCM) in [24]. If the residual inductor current is positive (towards the load), then a low-side body diode will conduct (through $M_{4,5}$), forcing V_x negative. However, if the current is negative, the switching node will be charged by the residual inductor energy, eventually resulting in body diode conduction through M_8, M_7, and $M_{1,2}$. In principle, for a fixed deadtime duration, the magnitude of the negative current can be used to charge the switching node to a level that approximates zero-voltage switching (ZVS) for the low-high V_x transition.

To get an approximate ZVS transition at the end of states C and D, the ZCD scheme uses a single 5V inverter to measure the state of the switching node. The inverter switching threshold



State and Switch Sequence

State	Time	$M_{1,2}$	M_3	M_4	M_5	M_6	M_7	M_8
A	t_1	on	on	on	off	off	off	off
C	t_2	off	off	on	on	off	off	off
B	$2t_1$	off	off	off	on	on	on	on
D	t_3	off	off	on	on	off	off	off

Fig. 3 Circuit States with inductor current waveforms and switching sequence.

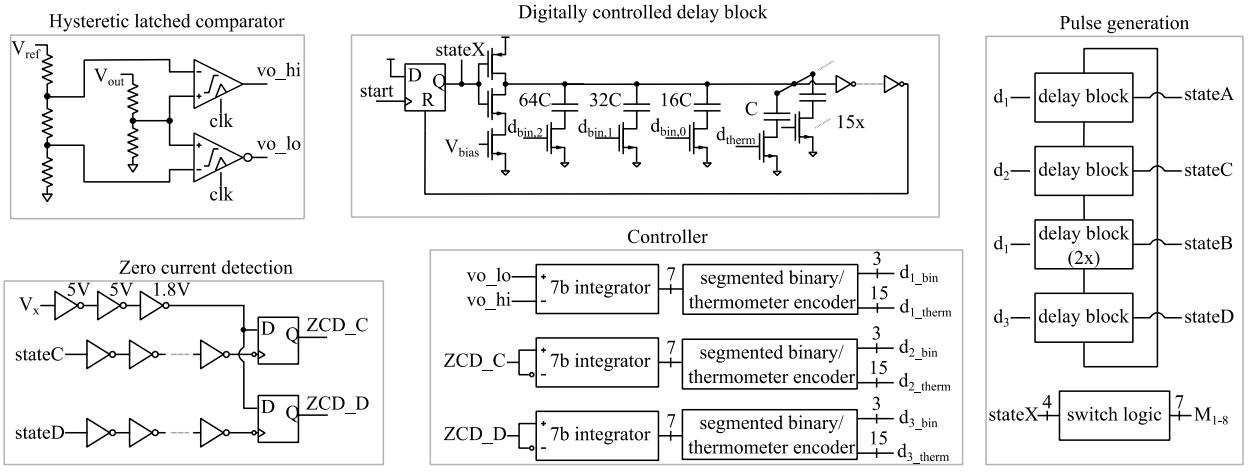


Fig. 4 Illustration of control and pulse generation circuit blocks.

is skewed to approximately 4.0 V such that if the inverter registers a '0', this corresponds to a switching node voltage, V_x < ~4.0 V; if the inverter registers a '1', this corresponds to V_x > ~4.0 V. The state of the 5 V inverter is sampled synchronous with the signal connected directly to the gates of M_4 and M_5 to minimize the effect of propagation delay through the ZCD chain. The state is held with a digital latch for the duration of the clock period. Time intervals t_2 and t_3 are then adjusted through two nested 1-bit integral control loops that act on d_2 and d_3. These time intervals are updated at a frequency of $f_{sw}/2$ to provide sufficient settling time and ensure stability of the loop. For example, if the switching node registers *high* during either state, the corresponding time interval is decreased incrementally; the opposite action is taken if the switching node registers low (below the inverter threshold). The control system thus acts to regulate the switching node voltage near the skewed inverter threshold of ~4 V, allowing the residual inductor energy to pre-charge the switching node, reducing loss due to parasitic capacitance on V_x.

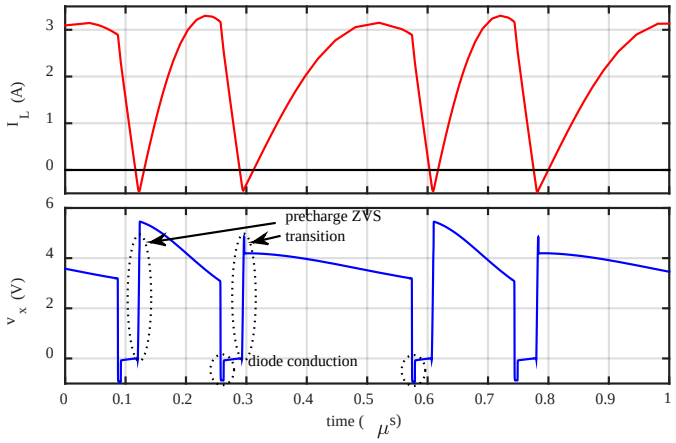


Fig. 5 Example inductor current and switching node voltage with regulated ZCS (cadence simulation)

Fig. 5 shows a cadence simulation of the inductor current and switching node voltage with the ZCD regulation active. On the low-high transitions, the switching node is precharged to around 4-5 V before the next switching state is engaged. This is accomplished by allowing a slightly negative inductor current after states C and D. As implemented, there is no zero error bin for the ZCD scheme, therefore, the process will result in limit cycling around the zero current state. In extracted simulation, the limit cycle magnitude is < 50 mVpp on node V_x and less than 25 mA in the inductor current level, thus it has negligible impact on the voltage and current waveforms or efficiency. It should be noted that achieving ZVS on the hard-switching transitions was not achieved in this design. This was in part because it would require tuning the deadtime after states A and B as the load current changed, as in [25]. Also, for load currents > 1 A, the required deadtimes are less than 300 ps; this was not straightforward to implement reliably in the series-parallel design due to the many floating devices and challenge in time alignment of the gate signals. Therefore, up to 5.0 ns of body diode conduction was allowed in the deadtime following states A and B, which did degrade efficiency somewhat, but ensured a margin of safety on the deadtime duration to prevent cross conduction across process and temperature variation.

The basic structure of the control and pulse generation is also shown in Fig. 4. Regulation of the output voltage is implemented through a hysteretic sampled comparator with a 1% (~40 mV) zero-error bin (i.e. a 1.5-bit flash ADC). Digital integral control operates on the single control variable, d_1, which regulates time period t_1 (state-A). Due to symmetry in the series-parallel architecture, state-B is hard-coded to be twice the duration of state-A. Primarily this ensures that the peak of the current waveform in states A and B is the same, while reducing control complexity to a single variable. It should be noted that variation in the timing of state A and B results only a very minor impact on efficiency due to higher RMS/DC current ratio.

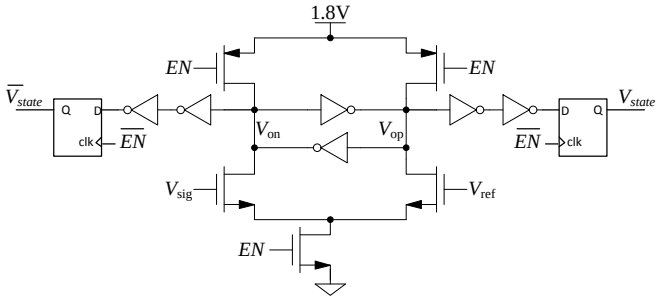


Fig. 6 Sampled comparator schematic

The 1-bit integral control scheme operates with a simple increment or decrement of duty cycle, d_1. The output voltage is sampled at the switching frequency and multiple samples are averaged to determine the direction of the feedback correction. The maximum update rate occurs at $f_s = f_{sw}/2$, corresponding to two averaged samples. An additional ~1.5 MHz lowpass filter (not shown) is included on the feedback signal to reduce aliasing of the voltage ripple, extraneous triggering in the control block, and to absorb kickback from the sampled comparator. Fig. 6 shows the circuit implementation of the sampled comparators used for the voltage-mode controller. The comparator operates in a reset phase when *EN* is low. When *EN* is high, the comparator latches in the state of the output voltage relative to a reference. The latched state is held until the next sampling phase by a secondary d-flip-flop that holds the value during the reset interval.

Timing of the sequential states A-D and respective duty cycles is controlled by a sequence of matched delay blocks. Each delay block includes a current-starved inverter with a variable capacitive load, as shown in Fig. 4. To simplify routing and encoding, the design uses three binary weighted control bits and 15 thermometer encoded capacitor loads. Each sequential delay block is configured to start the following timing interval and reset its own state. This provided a simple means to set the duration of each duty cycle, with state B encoded to twice the duration of state A. Importantly, while matching among delay blocks is beneficial, it is not critical as each block can be individually tuned. Matching internally within each block was improved through careful layout, but mismatch on the block level is only a problem in terms of absolute resolution of each

duty cycle (i.e. effective number of bits). The use of a variable capacitor load can be appreciated as similar to other works which used binary or thermometer weighted delay cells, [26], [27]. However, the advantage of using a tunable load is that it does not require a multiplexor or combinational logic to reconstruct the gating signal. This helps to eliminate parasitic delays and latencies in the path of the switching signal.

B. Powertrain, gate drivers, and level shifters

The nominal 3:1 series-parallel integrated circuit (IC) was designed in a 180 nm bulk CMOS process with a 5 V option for power devices. The process also supported triple-well junction isolation, which was used for power devices and many of the floating analog blocks. The design used an all n-channel power train and gate drivers with on-chip bootstrapping to drive the gates above their respective source terminals. The level shift and bootstrapping circuit shown in Fig. 7(a) was used for all devices. In order to ensure relative uniformity of propagation delays for all switches, and reduce asymmetry in the turn-on and turn-off timing intervals, the level shifter used a linear OTA structure, instead of a latching structure.

The differential level shifter used 15V LDMOS devices ($M_{xa,b}$) to steer current into diode connected 5V PMOS devices. Signals V_a and V_b drive a simple OTA with a gain of 30-40dB to recover the drive signal at a floating (bootstrapped) common mode level. This signal is then passed to a 5V inverter chain that scales up in size to drive the respective switching device. To reduce latency without using appreciable DC bias current, the differential pair, $M_{xa,b}$, is degenerated with an RC network. The capacitor provides a feedforward zero to provide a pulse of current in the switching interval and speed recovery of the floating drive signal. Resistors R_s and R_d limit the DC bias current that remains for the duration of the switching state.

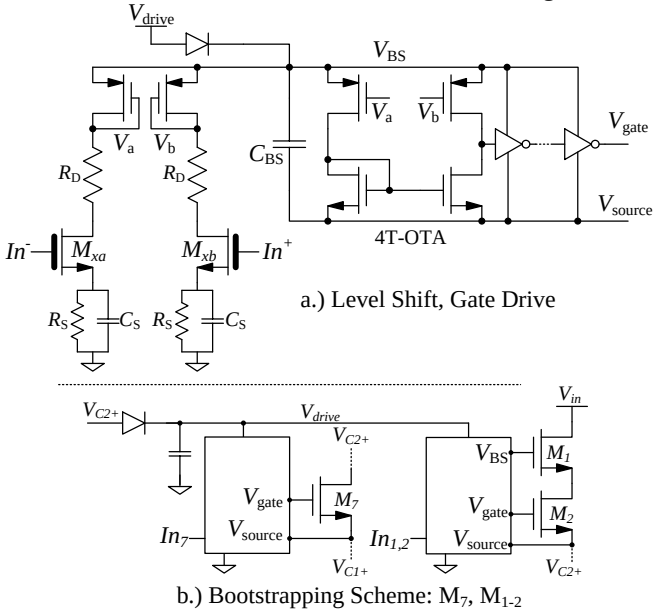


Fig. 7 Level shift, gate drive, and bootstrapping circuit

Bootstrapping was achieved using an isolated deep n-well diode with a 15V breakdown and bootstrap capacitor, C_{BS} for each switch. The same structure was used for M_4-M_6 with V_{drive} = V_{out} as these are all ground referenced in at least one phase. Device M_5 also used the same level shift circuit to maintain symmetry even though in principle it is ground referenced in all phases. Devices M_3 and M_8 were bootstrapped from V_{C1+}, the floating potential at the top plate of C_1. Devices M_7 and $M_{1,2}$ required a different scheme, shown in Fig. 7(b). These devices used the potential, V_{C2+}, from the top plate of C_2. However, this required nested bootstrapping with a single rail created by rectifying the peak V_{C2+} potential and using it as the V_{drive} voltage for M_7 and $M_{1,2}$. To create the bias voltage for the cascoded device, $M_{1,2}$, the gate of M_1 was connected to the V_{BS} potential in the respective level shift circuit. This ensured that the drain-source voltage of M_2 never exceeded 5V in any operating phase.

For startup purposes and to ensure that each bootstrap capacitor reaches the correct steady state value, the precharge circuit in Fig. 8(a) was used to initialize the voltage of each bootstrap capacitor in the circuit. A floating voltage reference was created by using diode connected devices. These included a 15V LDMOS and a 5V inverter to match the potential needed for the eventual gate drivers. A source follower circuit used a matched 15V LDMOS to precharge the bootstrap capacitors to just over the threshold voltage of the 5V inverter. Because during normal operation, the bootstrap voltage equilibrates at a voltage higher than the precharge level, the precharge circuit automatically turns off and does not draw power from the supply.

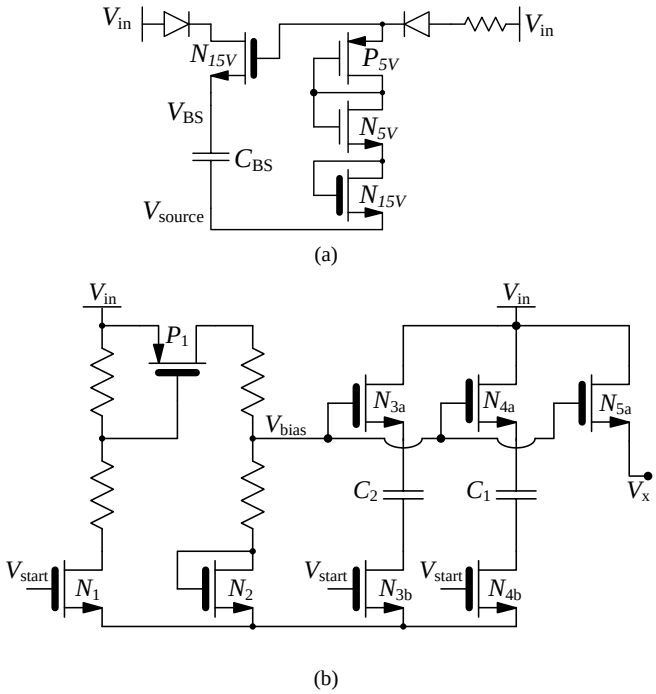


Fig. 8 Startup circuit (a) for bootstrap capacitors, and (b) for flying capacitors and switching node

A secondary precharge circuit was used for flying capacitors and the switching node, Fig. 8(b). This circuit was initialized during a startup phase with the load disconnected and all power devices are off. When signal V_{start} is high, device N_1 turns on,

pulling the gate of P_1 low, and charging node V_{bias} to approximately $V_{in}/3$ + threshold voltage of N_2. Devices N_{3b} and N_{4b} discharge the bottom plate of flying capacitors C_1 and C_2. Devices N_{3a} and N_{3b} simultaneously charge the flying capacitors to approximately $V_{in}/3$, with their threshold drop compensated by N_2. The switching node is charged by device N_{5a}; with the inductor in place, this serves to also charge the bypass capacitor, C_o, preventing overcurrent scenarios when the circuit starts switching after the startup phase. Importantly, when the startup signal, V_{start}, is low, the precharge circuit turns off, thus there is no residual impact during normal operation.

V. EXPERIMENTAL RESULTS

Similar to the assembly technique used in [28], the IC was flip-chip bonded directly to a printed circuit board (PCB) for testing. In contrast to [28], this implementation uses off-chip flying capacitors which introduces additional challenges. The parasitic inductance introduced by the interconnect to and from the off-chip flying capacitors can lead to high-frequency ringing after hard-switching transitions. Since quasi-resonant operation introduces two hard-switching transitions in this design, it is critical to minimize parasitic inductance to prevent voltage breakdown of switching devices from parasitic ringing. In order to reduce the ringing amplitude, 6 nF of flying capacitance was placed on-chip as MIM capacitors in parallel with the off-chip capacitors. Additionally, the PCB layout used the interconnect structure shown in Fig. 9 with a thin dielectric. Blind vias with a dielectric thickness, t = 3.7 mil 0.1 mm) were used to reduce the parasitic loop inductance as much as possible. Compared to an alternative layout with flying capacitors on the bottom of the PCB, the loop area (and approximate parasitic inductance) was reduced by around 3x, assuming a 20 mil (~0.5 mm) thick PCB.

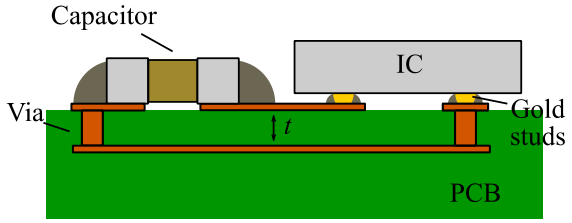


Fig. 9 Drawing of low-inductance PCB assembly of the IC with flying capacitors.

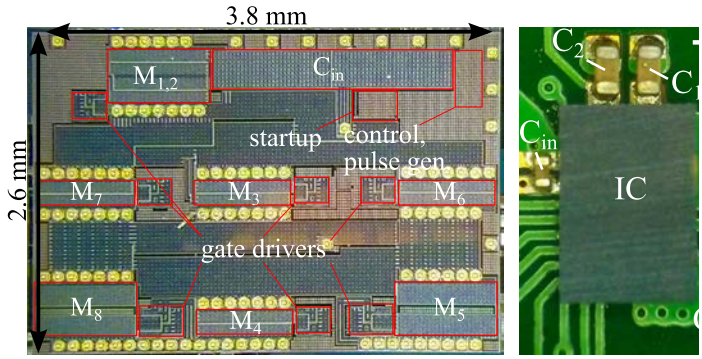


Fig. 10 Photographs of the IC and PCB flip-chip assembly

Fig. 10 shows photographs of the die and the printed circuit board with the flip-chip assembled IC and passive components. The die is 3.8 mm by 2.6 mm and includes gold stud terminations to connect to each of the flying capacitors, the switching node, ground, V_{in}, and various control signals. Each of the switches and respective gate drivers are shown to highlight their relative die area. As the control and startup blocks consume relatively small die area, the remainder of the die area is used for bootstrap, bypass, and extra flying capacitance.

Off-chip flying capacitors are 0402 components with a nominal/derated capacitance of 470/330 nF. Input and output bypass capacitors are 0201 and 0402 respectively with nominal values of 0.22 and 4.7 µF. The inductor value is 36 nH and is also an 0402 footprint (*Coilcraft, PFL1005*). The thickness (height) of the solution is ~1.0 mm including the 20 mil PCB (the thickness being limited by the 0402 components). The total volume (bounding box) of the converter is less than 20 mm^3, including the thickness of the PCB.

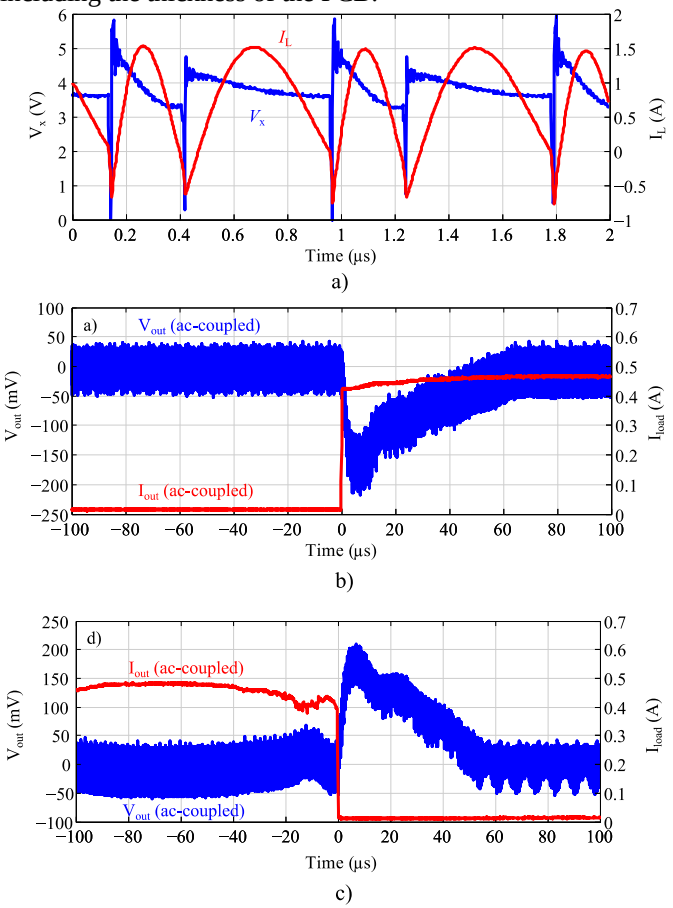


Fig. 11 Measured inductor current and switching node voltage at 1 A load current (a), measured converter response to a 0.5 A load current step (b), and response to unloading step (c).

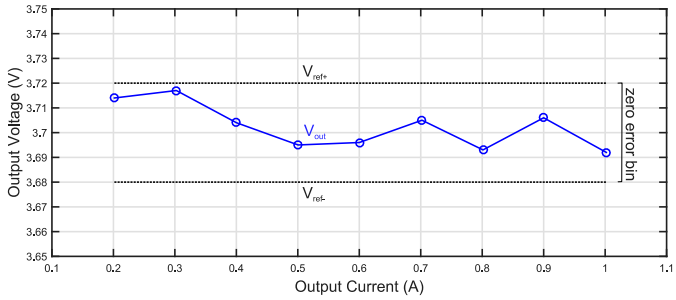


Fig. 12 Steady-state regulated voltage levels

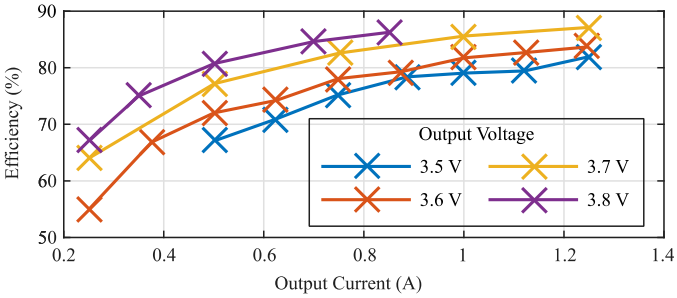


Fig. 13 Measured converter efficiency for different output voltages

Fig. 11(a) shows measured switching voltage (V_x) and inductor current waveforms at a load current of 1 A and an output voltage of 3.7 V. The inductor current is estimated (integral of the V_x - V_{out}) because the solution did not afford a method to directly measure I_L due to the compact size, but the resulting body diode conduction pattern indicated effective detection and regulation of the zero current switching state. Here, waveforms show effective operation of zero current detection within the detection window and inductor waveforms in quasi-resonant operation.

Fig. 11(b) shows effective operation of the control scheme; the output voltage is effectively regulated into the 20 mV zero error bin. For a load current transient of 0.5 A, the integral feedback controller settles in 60 µs. A similar settling time is achieved for the unloading transient shown in Fig. 11(c). Fig. 12 shows the steady-state regulated voltage levels for a load current range between 0.2 A and 1.0 A. It can be seen that across this range, the converter regulates the output voltage inside the zero error bin of 3.7 V ± 20 mV. The transient response of the controller is relatively slow due to the 1-bit integral control scheme, and because the maximum update rate of the controller is $f_{sw}/2$. In Fig. 11(b)-(c), the switching frequency was ~1.7 MHz (it was slightly higher than in Fig. 11(a) due to higher load current). However, it can be appreciated that the control bandwidth could be improved in future designs with higher quantization resolution of the voltage-mode instrumentation and a more complex PID control scheme. The goal in this work was to demonstrate some form of feedback regulation that worked in concert with nested zero-current detection, and in this regard, the design was successful.

Shown in Fig. 13, efficiency of the converter is measured at 87.5 % for 3.7V output, 12 V input and 1.2 A load current. There is slight efficiency degradation at lower voltage setpoints due to higher rms/DC current ratio and higher switching frequency.

Table I shows a comparison with previous work [20], [29]–[31]. This work shows high absolute power (4.6 W) and power density compared to previously published designs. The total volume of the solution is less than 20 mm^3 with the use of only 0402 and 0201 capacitors and a mm-scale (roughly 0402 footprint) 36 nH inductor. Importantly, this work shows that the series-parallel topology is both viable and promising for use as a hybrid switched capacitor converter. While there is a need to develop methods for gate driving with the many floating devices, this can be accomplished with an effort to develop means for startup and bootstrapping from flying nodes. A startup (precharge) circuit is also important for a robust design. There are further opportunities to improve the control and regulation. In particular, the feedback regulation method presented here was limited in terms of transient response due to the relatively simple integral control method, but there are few roadblocks to implementing faster control algorithms in future implementations.

Overall, this work presents the first near-monolithic implementation of a hybrid-class series parallel converter. Much of the discussion and details presented for this converter are extensible to higher conversion ratio prototypes and other architectures such as Dickson and multilevel converters.

TABLE I. COMPARISON WITH PREVIOUS WORK

	[29]	[30]	[31]	[20]	This work
Topology	6:1 SC	R^{2}SC	3-level	2:1 ReSC	3:1 ReSC
Process	160 nm	180 nm	130 nm	180 nm	180 nm
In./Out. (V)	16/3.3	1.8/1.2	2.4/1.2	6/3	12/3.7
Feedback	yes	no	yes	no	yes
Cap. Tech.	ceramic	MIM	MOS	MIM	Ceramic
Cap. Size	1 µF	3 nF	18 nF	24 nF	330 nF
Inductor (nH)	-	5.5-18	1	1.1-5.5	36
Power (W)	0.112	0.84	1	7.7	4.62
Size* (mm^3)	1.1	0.5	2.5	21	20
PD (W/mm^3)	0.10	0.17	0.5	0.37	0.23
Eff. @ PD	70 %	69 %	63 %	85 %	87 %

*volume of bounding box

VI. CONCLUSION

Hybrid, resonant, and soft-charged switched capacitor converters are increasingly promising to address the needs of future high-density power delivery applications. This paper explored the use of the series-parallel architecture, its capability to operate in resonant and quasi-resonant modes, and methodologies to implement variable regulation in a small form-factor integrated circuit prototype. A modified architecture was presented that can operate with single voltage rated switches without impacting the VA rating of the converter. A simplified method for implementing closed-loop control was presented that uses nested zero-current detection and regulation. Several IC implementation details were discussed including a new level shift circuit, a bootstrapping scheme for floating power switches, and startup circuitry to precharge bootstrap capacitors.

Load-step testing confirmed that the implemented control scheme is capable of closed-loop regulation with settling times of 60 μs for a 500 mA load step. Peak converter efficiencies of 82 % to 87 % were achieved for output voltages between 3.5 and 3.8V. While the output voltage range of the converter was limited, this design demonstrated that closed loop regulation without the need for manual frequency tuning is possible hybrid-class SC converters operated in quasi-resonant modes.

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