Developing robust fabrication of Si/SiGe quantum dots with integrated RF-SET charge detectors

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Abstract

Solid-state approaches to quantum computing include quantum dot qubit implementations based on the Loss-DiVincenzo proposal. Prior work in GaAs two-dimensional electron gas (2DEG) materials serves as a proving ground for device designs that can be ported to Si/SiGe 2DEG systems, where the coherence time of quantum information is longer due to a combination of physical effects unique to strained Si quantum wells. In spite of the promise of Si/SiGe quantum dot qubits, several materials issues can reduce successful device yield. This work presents results from the exploration of two of these issues: the reliability of ohmic contacts to the 2DEG and the leakage current from the metallic Schottky gates used to form the quantum dots. For the ohmic contacts, growth recipes with yields approaching 100% based on two different metallizations, Au/Sb and Ag/Sb, are presented in the context of a known model for diffusion and alloying in Si. Addressing the issue of leakage currents, experiments on devices fabricated at Dartmouth strongly suggest that the major source of current leakage arises from the region near the etched mesa sidewall, where the photolithographically created metallic Schottky gate leads cover the edge of the device mesa. The solution presented here involves the deposition of SiO_2 as a barrier oxide between the gate metallization and the underlying etched region to block whatever current paths might exist between the edge of the mesa and the 2DEG. Two variations on this theme are discussed: the deposition of oxide beneath the large gate leads only and the deposition of oxide immediately after etching to partially backfill the etched region with insulator. Results suggest that the latter method holds the most promise and may work even better with more robust insulators. Finally, the results of several successful devices are presented, including an radio-frequency single-electron transistor on Si/SiGe 2DEG material and a quantum dot formed in a Si/SiGe 2DEG using gates with barrier oxide underneath. This work concludes with a discussion of future directions suggested by the results obtained thus far and based on progress already made along those directions.

Acknowledgements

Text to come later...

Contents

Abstract ii

Acknowledgements iii

Table of Contents iv

List of Tables vii

List of Figures viii

1 Introduction and Motivations **1**

1.1 Solid state Approaches to Quantum Computation 2

1.2 Prior Results in GaAs 5

1.3 Motivations for Si/SiGe 6

1.4 Robust Device Fabrication 7

1.5 Outline 7

2 Theoretical Background **9**

2.1 Two-Dimensional Electron Gas (2DEG) 9

2.2 Mesoscopic Transport in One Dimension 10

2.3 Quantum Point Contacts 14

2.4 Quantum Dots 16

2.5 The Radio-Frequency Superconducting SET as a Charge Sensor 21

3 Experimental Methods **25**

3.1 Device Patterning 25

3.1.1 Photolithography 25

3.1.2 Electron Beam Lithography 29

3.2 Material Growth and Deposition 32

3.2.1 Si/SiGe Heterostructure 32

3.2.2 Thermal Evaporation 33

3.2.3 Electron Beam Evaporation 37

3.2.4 Shadow Evaporation 39

3.2.5 Ohmic Contact Growth 41

3.3 Material Removal 43

3.3.1 Wet Etching 43

3.3.2 Reactive Ion Etching 45

3.4 Cryogenics 49

3.4.1 Liquid Helium Immersion 50

3.4.2 Dilution Refrigerator 51

3.4.3 Heliox AC-V Refrigerator 53

3.5 Measurements 56

3.5.1 Static Protection and Wirebonding 56

3.5.2 DC and Low Frequency Electronics 58

3.5.3 RF Electronics 61

4 Si/SiGe Materials Issues #1: Ohmic Contacts **62**

4.1 Alloying and Diffusion in Si/SiGe 64

4.2 Approach #1: Au/Sb Alloy 66

4.3 Approach #2: Layered Cr/Sb/Ag 67

4.4 Approach #3: Layered Au/Sb/Au 71

4.5 Summary 72

5 Si/SiGe Materials Issues #2: Leakage Current 74

5.1 Problem Background 74

5.2 Approach #1: Layered Schottky Gates 77

5.2.1 RIE removal of SiO2 81

5.3 Approach #2: Backfilled Etch 82

5.4 Summary 86

6 Devices in Si/SiGe 88

6.1 RF-SET on Si/SiGe 88

6.2 QPCs in Si/SiGe 90

6.3 QDs in Si/SiGe 95

6.4 Integrated QD/SET and Double QD systems in Si/SiGe 99

6.5 Summary 100

7 Summary and Future Directions 102

7.1 Summary 102

7.2 Conclusions 103

7.3 Future Directions 104

A Step-by-Step Device Fabrication 105

List of Tables

1.1 DiVincenzo Criteria 2

3.1 Si/SiGe heterostructure material grown at University of Wisconsin - Madison 33

3.2 E-beam Evaporation Crucible Guide 39

3.3 RIE Recipes 49

4.1 Ag/Sb Ohmic Contact Annealing 69

5.1 Performance of Devices Without Barrier Oxide 77

5.2 Performance of Devices With Oxide Underneath Gates 79

5.3 Performance of Devices With Backfilled Etch 86

List of Figures

1.1 Schematic of the Loss-DiVincenzo proposal 4

2.1 Schematic diagram of Si/SiGe 2DEG material, including both energy band diagram and growth profile. 11

2.2 A 1-D barrier in the middle of a Fermi sea of electrons with voltage bias V applied across the barrier. 12

2.3 (a)Schematic diagram of split-gate QPC and (b) conductance steps of an idealized QPC [1]. 15

2.4 Schematic diagram of a quantum dot with weakly coupled source and drain leads. . 16

2.5 Schematic diagram of a QD potential under Coulomb blockade (a) and single particle tunneling (b), (c). 19

2.6 Schematic diagram of ideal Coulomb blockade oscillations in an QD. 20

2.7 Schematic of an SET embedded in an RLC tank circuit functioning as a charge detector. 22

2.8 Cartoon of RF-SET performance illustrating hypothetical $I - V$ (a) and reflected coefficient (b) curves for in (solid) and out (dashed) of Coulomb blockade. 24

3.1 Schematic diagram of the photolithography process. 27

3.2 Schematic diagram of the e-beam lithography process. 30

3.3 Schematic diagram of the SEM apparatus for e-beam lithography. 31

3.4 Simplified schematic of the Si/SiGe heterostructure. 34

3.5 Schematic diagram of a thermal evaporator. 36

3.6 Schematic diagram of the source apparatus from the e-beam evaporator. 38

3.7 Schematic diagram of the shadow evaporation process. 40

3.8 (a) Schematic of the RIE apparatus. (b) RIE process on a sample. 46

3.9 AFM image of results from an improperly tuned process. This etch recipe should have yielded an etch depth of 100±15 nm, yet it produced features an order of magnitude deeper. 48

3.10 Schematic diagram of a basic dunker apparatus. 50

3.11 Schematic diagram of a dilution refrigerator. 52

3.12 Schematic diagram of the Heliox AC-V refrigerator. 55

3.13 Schematic diagram of apparatus for measuring DC leakage currents. 59

3.14 Schematic diagram of apparatus for 4-probe conductance measurements. 60

3.15 Schematic diagram of RF setup. 61

4.1 Illustration of the three different ohmic contact metallization profiles. 63

4.2 Optical micrograph of Ag/Sb ohmic contact surface, post-annealing. Samples annealed at 600°C for 30 minutes always exhibited this surface appearance when the ohmic contacts worked properly. The $\sim 5\mu$m square pit feature on the left side gives an idea as to the scale. 70

4.3 Optical micrograph of Au/Sb ohmic contact surface, post-annealing. Samples annealed at 400°C for 4 minutes routinely exhibited this surface appearance. The width of this field of view is approximately 90 μm. 72

5.1 (a) Leakage current data from a typical device without barrier oxide. (b) Lithography profile for these early devices. (c) Etch profile from [2]. 76

5.2 Diagram illustrating the lithography involved in creating Schottky gates with a layer of barrier oxide underneath. The SiO_2/Ti/Pd sandwich is fabricated using photolithography, and each successive layer of Pd represents an e-beam lithography step. 78

5.3 (a) Leakage current data from a typical device with barrier oxide deposited as part of large Schottky gate lead metallization. Each trace represents a different gate. These gates were not exposed to e-beam irradiation. (b) Optical micrograph of lithographic error on a different device, where the viewing window for the alignment marks overlapped the edge of the ohmic lead, resulting in leakage. The width of the device mesa is this figure is approximately 20 μm. 80

5.4 Important differences in oxide removal: (a) BOE removes SiO_2 isotropically, eating away the oxide under the gates, while (b) RIE is highly anisotropic, leaving the barrier oxide mostly intact while removing the native oxide. 81

5.5 AFM scans and profile sections illustrating the results of the RIE removal of SiO_2. . 83

5.6 Diagram illustrating the lithography involved in creating Schottky gates atop a backfilled barrier oxide deposited immediately after the etch step. The SiO_2/Ti/Pd sandwich is fabricated using photolithography, and the subsequent layer of Pd represents an e-beam lithography step. 84

5.7 Leakage current data from a typical device with barrier oxide deposited immediately after the RIE step that defines the device mesa. Each trace represents a different gate, and those gates that leak were all subjected to e-beam irradiation in subsequent lithography steps. 85

6.1 SEM micrograph of RF-SET fabricated on SiGe. This is a picture of the actual device measured. 89

6.2 DC performance of the SET with R_N = 215 kΩ showing the superconducting I-V curve and Coulomb blockade oscillations. 91

6.3 RF performance of the SET showing (a) reflected power in (red) and out (blue) of Coulomb blockade as well as (b) the modulation of the 1.02 GHz carrier wave with a 100 kHz 0.3e signal applied to the capacitively coupled gate. 92

6.4 Plot of the conductance vs. gate voltage behavior of a typical QPC device without barrier oxides under the gates. Red and blue traces represent two different QPCs on the same device with a common gate between them. Leakage current noise overwhelms the pinch-off behavior below $V_g \approx -1.4V$. 93

6.5 Plot of the conductance vs. gate voltage behavior of a typical QPC device with barrier oxides under the gates. Red and blue traces represent two different QPCs on the same device with a common gate between them. This device exhibited leakage current behavior in the dot-forming gates for $V_g < -2.75$, due to the e-beam exposure of the thin (5 nm) barrier oxide at the mesa edge. 94

6.6 Leakage current performance; a small offset in the current amplifier is responsible for the non-zero baseline seen in (a) and the shifting baseline seen in (b). 96

6.7 QPC performance. Device 5/11 failed to show pinch-off due to leakage currents caused by lithographic errors. Device 5/4 shows pinch-off in spite of the large leakage current on gate 18 97

6.8 (a)CBO in a Si/SiGe quantum dot formed by Schottky gates with barrier oxides underneath. (b)Repeatability in successive measurements (blue) was strong, apart from a small offset in gate voltage (≈ 0.185 V, already corrected in the plot). 98

6.9 SEM micrograph of a combined SET/QD device on Si/SiGe. This is a picture of the actual device that exhibited Coulomb blockade oscillations in the dot. In spite of appearing intact, the SET measured as an open-circuit. 99

6.10 SEM micrograph of a double QD device pattern fabricated as part of a dose array on scrap material. Using dose arrays, a reliable lithography recipe for producing these double QD patterns was obtained. 100

Chapter 1

Introduction and Motivations

Realization of a viable quantum computer has become one of the most hotly pursued goals in the recent history of several diverse areas of physics research, and for good reason: the inherently quantum nature of the information processed by a quantum computer would enable an entirely new approach to computing. In addition to their broadly appealing capability of reducing the complexity (and therefore computing time) of certain types of classical computing problems, quantum computers could permit exact simulations of real quantum systems at useful time scales, by virtue of being quantum systems themselves. The physical form of a quantum computer depends on which candidate system serves as its essential element, the quantum bit or qubit. Candidate qubits range from ensembles of spins in liquid state nuclear magnetic resonance (NMR) systems to single spin qubits such as ions in magento-optical traps or electrons in a variety of solid-state systems. [3, 4] The following work will discuss the issues surrounding and progress made towards the development of a reliable version of one such candidate solid-state qubit system: a quantum dot in a Si/SiGe heterostructure with integrated charge detection. This first chapter highlights the motivations for this particular solid-state system in addition to providing an outline of the chapters that follow.

Table 1.1 DiVincenzo Criteria

1. Two-level Systems	Information must be encoded as a qubit, a quantum two-level system, such qubits must be scalable to usable register sizes and stable enough to perform computations
2. Initialization	Each qubit should be initializable: each qubit must be reset to its ground state at the start of each computational cycle
3. Isolation	Interactions with the environment must be minimized to reduce the loss of quantum information to decoherence effects; computation speeds should be $\sim 10^4$ faster
4. Logic Gates	Logic gate implementation requires the Hamiltonian of each qubit and the interactions between qubits to be independently controllable
5. Readout	Measurements determining the state of each qubit should be fast, highly efficient, and very reliable; readout of each qubit must be independent

1.1 Solid state Approaches to Quantum Computation

Of all the candidate qubit systems under investigation, solid-state systems hold perhaps the greatest appeal, for reasons both physical and practical. The five DiVincenzo criteria provide a convenient evaluation metric for any candidate qubit system. [3, 5]

Physically speaking, solid-state systems are advantageous, since they allow the experimenter to engineer a broad array of different parameters. This provides a degree of tunability unavailable in

other candidate qubit systems where more parameters are intrinsically fixed, such as in the case of the electronic structures of the ions used in magneto-optical traps and the molecules used in liquid-state NMR experiments. [3, 4] Whether the solid-state system in question is a semiconductor or a superconductor, the relevant energy scales are readily designed to produce the required quantum two-level systems with controllable Hamiltonians. Additionally, initialization control is readily achievable through several mechanisms, while the readout mechanisms available in solid-state devices include the fastest and most sensitive detectors of charge and flux. [4–7] Two of these devices, the quantum point contact (QPC) and the radio-frequency single-electron transistor (RF-SET), will be further discussed in the context of this work in later chapters.

In spite of these advantages, there are trade-offs inherent to solid-state candidate qubit systems: they necessarily suffer from the effects of strong interactions with their environment. Quantum information in the solid-state must therefore be stored and manipulated in forms that are relatively decoupled from the environment. Fortunately, by choosing to work with spin degrees of freedom in a semiconductor or by exploiting the energy gap in a superconductor, one can achieve solid-state qubits where the quantum information retains its fidelity on time scales sufficiently longer than that of the computation and readout processes. [4, 5] Reevaluating this discussion in the context of the DiVincenzo criteria, solid-state systems can be designed to readily meet criteria 1, 2, 4, and 5. Furthermore, solid-state systems can also fulfill criterion 3, given careful choice of how the quantum information is physically encoded and manipulated.

One particular proposal for semiconductor qubits merits additional consideration: the Loss-DiVincenzo proposal. Based on the well-developed methods of creating lateral quantum dots in semiconductor heterostructures, the details of which will be discussed later in this work, the Loss-DiVincenzo proposal uses the spin of a single electron on a quantum dot as the basis for a qubit. A complete set of logic gates arises from the combination of a “swap” gates governed by the exchange

interaction between electron spins on neighboring dots and single qubit rotations of spins on individual dots. [5,6] While a complete review of this proposal for solid-state quantum computing is beyond the scope of this work, one should note that recent advances in lateral quantum dot experiments have paved the way towards realization of the Loss-DiVincenzo proposal by demonstrating reliable readout [8–10], as well as controllable initialization and coherent spin manipulations. [11]

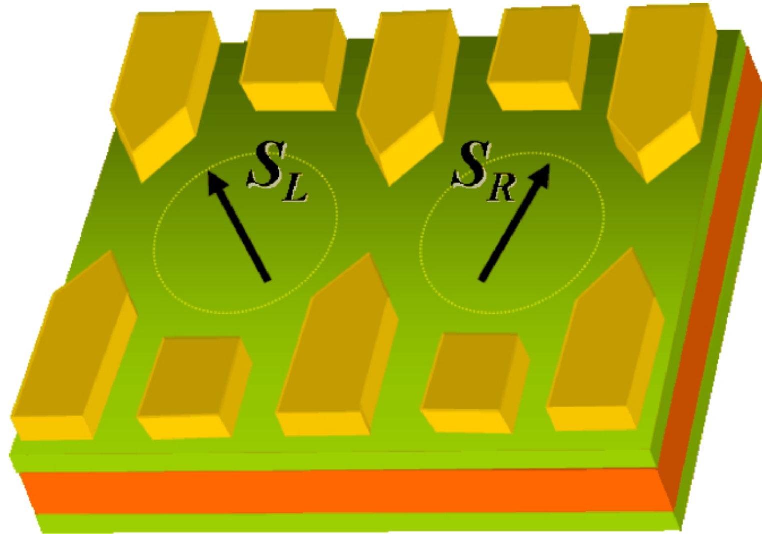


Figure 1.1 Schematic of the Loss-DiVincenzo proposal

Image courtesy Vitaly Golovach: http://theorie5.physik.unibas.ch/golovach/

Finally, speaking from a practical perspective, those solid-state proposals based on semiconductors possess powerful economic appeal. Most of the methods and materials required for device fabrication are well-known from the last half-century of the semiconductor industry. Also, the potential compatibility with current technologies remains quite high, particularly in the case of silicon-based qubits. Such technological synergy provides an additional advantage: easy scalability. The need for qubit systems that scale easily to the large register sizes needed for useful computation tends to be the most easily overlooked component of the first DiVincenzo criterion, yet it remains the critical one in terms of limiting the viability of a candidate qubit system. As a consequence of these economic

reasons and those physical ones already discussed, silicon-based semiconductor qubits represent one of the most promising solid-state approaches to quantum computation. [3, 4]

1.2 Prior Results in GaAs

As briefly mentioned above, the current state of progress towards Loss-DiVincenzo style qubits in lateral quantum dot systems includes successful demonstration of readout mechanisms and coherent spin manipulations. These results have been achieved in gallium arsenide (GaAs), a III-V semiconductor that can be readily grown as a heterostructure with aluminum gallium arsenide (AlGaAs) to produce the high-quality two-dimensional electron gas (2DEG) system needed for lateral quantum dot qubits. Readout mechanisms include capacitively coupled QPC and RF-SET charge detectors. [8, 10, 12, 13] The latest generation of these ultrasensitive charge detectors approaches the quantum limit [1, 14, 15], allowing for single-spin sensitivity when combined with spin-to-charge conversion schemes based on Pauli exclusion. [9, 16] Recent experiments also achieved initialization and coherent spin manipulation. [11]

These successes and the ease of fabricating high-quality GaAs/AlGaAs heterostructures certainly makes them the most convenient choice for developing lateral quantum dot qubits. In spite of that, the lifetime of spin information in GaAs-based qubits will likely remain shorter than that of Si-based qubits, as detailed below. As a result, long-term success in Loss-DiVincenzo style qubits will likely occur in Si-based systems, but GaAs devices remain an important proving ground for the techniques that will later be ported to Si devices. [4, 17]

1.3 Motivations for Si/SiGe

In addition to the compelling economic reasons for investigating Si-based quantum dot qubits already discussed, a number of unique physical properties also make Si systems a compelling choice. First and foremost, Si-based systems can be grown isotopically pure to insure that only the zero net nuclear spin species $^{2}8$Si is present, dramatically reducing the interaction between electron and nuclear spins, a large contributor to the decoherence of spin information in solid-state qubits. Spin-phonon interactions leading to spin relaxation represent another key mechanism that limits coherence times. Careful design of a lateral quantum dot system in the right Si heterostructure can reduce the effects of this spin relaxation mechanism, extending the lifetime of spin information. [17] Also, Si possesses a well-known six-fold valley degeneracy that produces strong spin mixing in the ground states, leading to increased electron-phonon interaction and decreasing the coherence time of spin information. Fortunately, introducing uniaxial compressive strain in a Si lattice partially lifts the valley degeneracy, decreasing spin-mixing as a a consequence. [17–20]

Better still, the creation of the quantum well in Si/SiGe 2DEG materials also benefits from growing a strained Si layer between SiGe alloy layers. By virtue of its higher atomic number, Ge has a larger lattice constant than Si, so its presence in the Si lattice results in an alloyed crystal whose lattice constant exceeds that of Si and scales directly with Ge concentration. Also worth noting is that Si exhibits a reduced spin-orbit coupling (SOC) interaction when compared to both GaAs and SiGe. Therefore, creating quantum dot qubits in 2DEG grown in a strained Si quantum will yield the longest coherence times. A more detailed discussion of the SiGe heterostructure required for such devices will be presented in later chapters. [4, 17, 19, 21]

1.4 Robust Device Fabrication

Initial efforts towards lateral quantum dots in Si/SiGe 2DEGs encountered several issues with reliability related to materials issues. As a relatively new materials system, Si/SiGe presents a variety of problems already solved in more mature systems, such as GaAs 2DEGs. One problem initially requiring further investigation was the growth of ohmic contacts to the 2DEG layer beneath the substrate surface. Early attempts met with low yields, so this work explores several approaches to developing robust techniques for growing ohmic contacts with collaborators from the University of Wisconsin-Madison, the results of which appear in chapter 4. Another issue that also merited thorough investigation was the presence of leakage currents arising from the Schottky gates required to form the quantum dots, since large leakage currents can easily overwhelm signal currents, reducing device yield dramatically. Chapter 5 of this document presents the results of a variety of different attempts to suppress this leakage current. [22–25]

1.5 Outline

Motivated by the reasons discussed briefly in this chapter, the following work will explore the basic theory behind the functioning of semiconductor quantum dots and, as well as the issues encountered while developing robust recipes for producing these devices in a Si/SiGe heterostructure. Chapter 2 discusses the theoretical background of charge transport through a variety of mesoscopic devices, including QPCs, quantum dots, and RF-SETs, as well as detailing how the RF-SET may be used as a charge sensor. Chapter 3 presents the wide array of experimental methods employed in this work, broken into several broad categories: device patterning, material growth and deposition, material removal, cryogenics, and measurements. Chapters 4 and 5 discuss the results of different approaches to solving the issues of growing reliable ohmic contacts and Schottky gates with reduced leakage

currents, respectively. Chapter 6 presents the data from successful RF-SET and quantum dot devices in SiGe, as well as the results of initial efforts towards integrating these devices. Chapter 7 concludes with summary statements and some discussion of directions for future exploration.

Chapter 2

Theoretical Background

This chapter presents a discussion of the essential theoretical background for the physics of mesoscopic devices, including 2DEGs, QPCs, quantum dots, and RF-SETs.

2.1 Two-Dimensional Electron Gas (2DEG)

High electron mobility at low temperatures can be achieved in Si-based heterostructures grown by ultrahigh vacuum chemical vapor deposition (UHVCVD), a process that allows for atomic layer precision growth of highly crystalline material. In the case of this material, the heterostructure includes both Si and SiGe, grown in specific combination to produce a strained Si layer containing a two-dimensional electron gas (2DEG). In addition to the benefits of strained-Si quantum wells highlighted in the previous chapter, growth of a quantum well with the right parameters can result in a lifting of the remaining two-fold valley degeneracy, with the measured valley splitting even exceeding the spin splitting when the correct combination of electrostatic and magnetic confinement is used. Quantum dots formed in Si/SiGe heterostructures provide the electrostatic confinement and external magnetic fields may be used to produce the magnetic confinement, with the adjustability

of both forms of confinement offering great control over the valley splitting. [20] Figure 2.1 depicts the growth profile of this material.

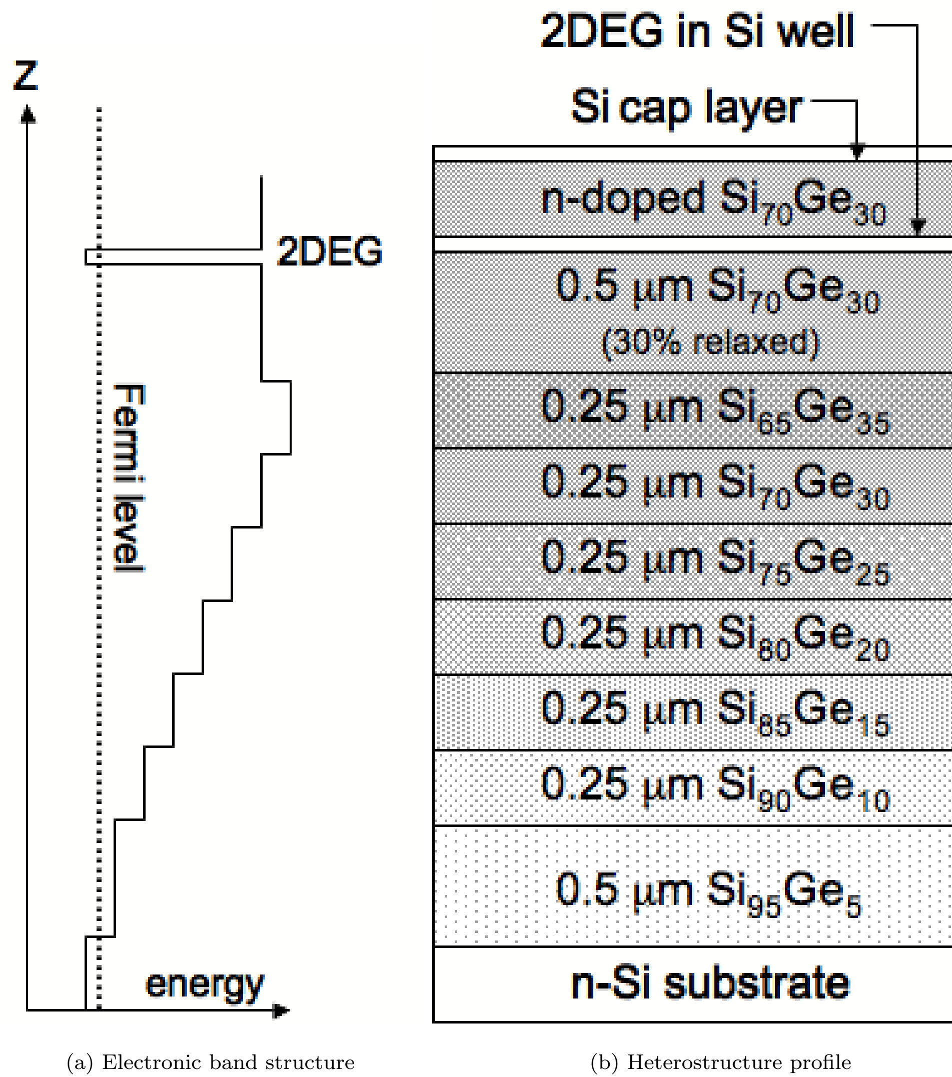
Beginning with the clean surface of a n-type Si wafer, growth of $Si_{1-x}Ge_x$ begins with step-graded layers increasing in concentration from $x = 0.05$ to 0.30 over several microns to allow for relaxation of the strain induced by the addition of Ge, which has a lattice constant $\approx 4\%$ larger than that of Si. Growing a layer of pure Si several nm thick atop this $Si_0.7Ge_0.3$ causes the Si lattice to stretch in the plane of the wafer, resulting in a uniaxial compressive strain of $\approx 2\%$ in the direction perpendicular to the surface. This strain, in addition to reducing decoherence processes as discussed in the previous chapter, provides the essential conduction band offsets relative to the surrounding $Si_0.7Ge_0.3$ required for a quantum well to form in the Si layer. After this strained Si layer, a layer of $Si_0.7Ge_0.3$ is grown, with modulation doping of P (an n-type dopant) occurring after 14 nm of additional growth to provide the charge carriers that will populate the 2DEG layer. Finally, the surface is capped with an additional Si layer a few nm thick. This final Si layer will naturally passivate with a thin layer of SiO_2 upon exposure to atmosphere. [19–23, 26–28]

2.2 Mesoscopic Transport in One Dimension

To begin with, one should consider a one-dimensional barrier in the middle of a Fermi sea of electrons with an applied voltage bias V, as depicted in Figure 2.2. The current through this barrier may be expressed as the sum of the currents flowing left-to-right and right-to-left. Current from the left lead is given by the following integral over all the states in k-space defined by the Fermi function $f[\epsilon(k), \mu_L]$:

$$I_L = 2e \int_0^\infty f[\epsilon(k), \mu_L] v(k) T(k) \frac{dk}{2\pi}. \tag{2.1}$$

$T(k)$ represents the transmission probability, and only values $k > 0$ are used to account for only left-to-right current flow. The factor 2 accounts for spin degeneracy, e is the electron charge, and



(a) Electronic band structure (b) Heterostructure profile

Figure 2.1 Schematic diagram of Si/SiGe 2DEG material, including both energy band diagram and growth profile.

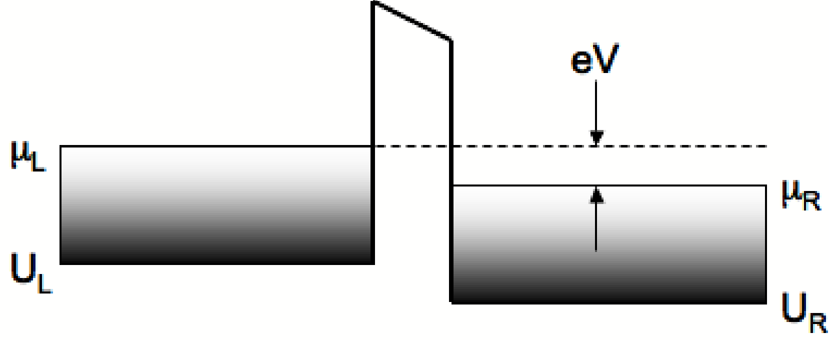


Figure 2.2 A 1-D barrier in the middle of a Fermi sea of electrons with voltage bias V applied across the barrier.

$v(k)$ is the drift velocity. Exploiting the chain rule allows for translation of the expression for current into terms of energy E,

$$dk = \frac{dk}{dE}dE = \frac{1}{\hbar v}dE. \tag{2.2}$$

Thus, the current integral becomes

$$I_L = 2e\int_{U_L}^{\infty} f(E,\mu_L)vT(E)\frac{dE}{2\pi\hbar v} = \frac{2e}{h}\int_{U_L}^{\infty} f(E,\mu_L)T(E)dE. \tag{2.3}$$

The velocity term cancels, consistent with the fact that there is a lower density of higher energy states with higher velocity. Similarly, the current from right to left can be expressed

$$I_R = -\frac{2e}{h}\int_{U_R}^{\infty} f(E,\mu_R)T(E)dE, \tag{2.4}$$

giving the total current as

$$I = I_L + I_R = \frac{2e}{h}\int_{U_L}^{\infty} [f(E,\mu_L) - f(E,\mu_R)]T(E)dE. \tag{2.5}$$

One should note that electrons whose energy falls between U_L and U_R do not contribute to the current, as there are no empty states available on the left side of the barrier to support propagation, allowing for the change in the limit of the integral.

Of particular interest is the current produced by applying a small bias voltage V around the Fermi level, small enough to allow for a Taylor series expansion of the difference in the Fermi level

$$f(E,\mu+\frac{eV}{2})-f(E,\mu-\frac{eV}{2})\approx eV\frac{\partial f}{\partial \mu}=-eV\frac{\partial f(E,\mu)}{\partial E}. \tag{2.6}$$

Therefore the current at small bias becomes

$$I=\frac{2e^2V}{h}\int_{U_L}^{\infty}-\frac{\partial f}{\partial E}T(E)dE. \tag{2.7}$$

In the small bias limit, the current and voltage are proportional, allowing the conductance $G=I/V$ to be expressed in terms of energy

$$G=\frac{2e^2}{h}\int_{U_L}^{\infty}-\frac{\partial f}{\partial E}T(E)dE, \tag{2.8}$$

yielding the quantum of conductance $G_0=\frac{e^2}{h}=38.7\mu\text{S}$ as a prefactor to the integral. The resistance quantum is merely the inverse of this value: $\frac{h}{e^2}=25.8\text{k}\Omega$. At very low tempratures, the Fermi function approaches a sharp step, allowing for the simplification $-\frac{\partial f}{\partial E}=\delta(E-\mu)$, reducing the conductance expression to

$$G=\frac{2e^2}{h}T(\mu). \tag{2.9}$$

Generally speaking, T represents a T-matrix with elements t_{mn} defined as the probability of electrons injected into the mode n ending up in the mode m, such that the total conductance can be expressed by summing over all the input and output modes. Furthermore, the Hermetian conjugate of the matrix $(t^{\dagger})_m n=(t)^*_{nm}$ allows for simplification of the expression

$$G=\frac{2e^2}{h}\sum_{m,n}|t_{nm}|^2=\frac{2e^2}{h}\sum_{m,n}t_{nm}t^*_{mn}=\frac{2e^2}{h}\sum_{m,n}t_{nm}t^{\dagger}_{mn}. \tag{2.10}$$

$$G=\frac{2e^2}{h}\sum_{m,n}(tt^{\dagger})_{nn}=\frac{2e^2}{h}Tr(tt^{\dagger}). \tag{2.11}$$

This concludes the outline of the Landauer formalism for conductance in 1-D that will inform the discussion of quantum point contacts that follows in the next section. [29–31]

2.3 Quantum Point Contacts

From the prior discussion of the physics of the 2DEG, the width of the quantum well is only a few nanometers and the energy spectrum for 2DEG electrons with respect to the z-direction (perpendicular to the surface) is discrete. Therefore, only the lowest subband in z is populated, allowing for simplification of the electron energy expression to 2-D,

$$E(k_x, k_y) = \frac{\hbar^2(k_x^2 + k_y^2)}{2m^*} \tag{2.12}$$

with m^* as the effective mass in Si, and x and y are directions parallel to the 2DEG layer. Given a density of electrons per unit area of $n(E) = \frac{m^* E}{\pi\hbar^2}$, the density of states $\rho(E)$ can be derived

$$\rho(E) = \frac{dn}{dE} = \frac{m^*}{\pi\hbar^2}. \tag{2.13}$$

Thus, the Fermi energy at low temperature is necessarily proportional to n_s, the sheet density of the 2DEG:

$$E_F = \frac{n_s}{\rho}.$$

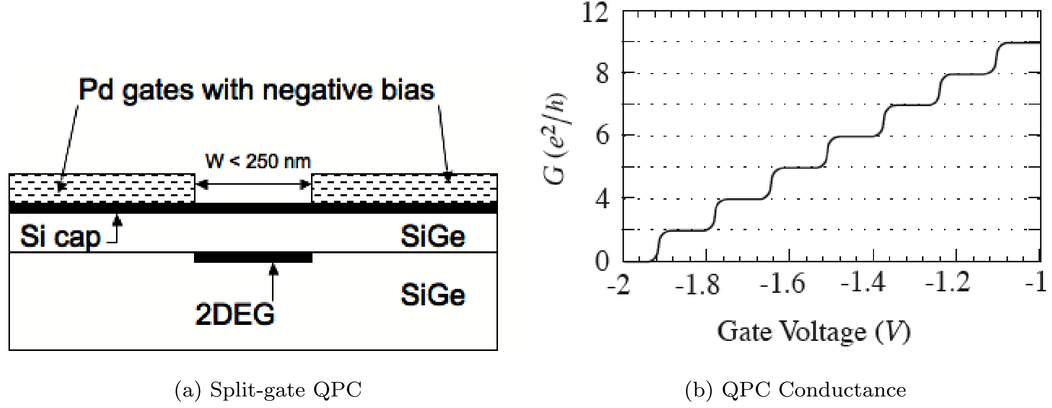
The sheet density can be used to understand the formation of constrictions in the 2DEG that constitute quantum point contacts (QPCs) by considering the effects off applying negative bias voltages to metallic Schottky gates fabricated on the surface of the material containing the buried 2DEG. A straightforward model based on capacitive coupling predicts the change in sheet density caused by a change in gate voltage V_g will be

$$\delta n_s = \frac{\epsilon\epsilon_0}{ed}\delta V_g, \tag{2.14}$$

where d is the distance between the surface and the 2DEG, e is the electron charge, and ϵ and ϵ_0 are the permitivities of SiGe and free space, respectively. Thus, a negatively biased surface gate can be used to deplete the 2DEG beneath, since the E_F varies linearly with V_g according to

$$\delta E_F = \frac{\epsilon\epsilon_0}{ed\rho}\delta V_g. \tag{2.14}$$

This ability to control the 2DEG population serves as the basis for the split-gate technique commonly used to form QPCs, combinations of which may then be used to form more complicated geometries like quantum dots.



(a) Split-gate QPC (b) QPC Conductance

Figure 2.3 (a)Schematic diagram of split-gate QPC and (b) conductance steps of an idealized QPC [1].

Within a QPC constriction like the one depicted in figure 2.3, the energy levels of the 2DEG become quantized in the direction perpendicular to the constriction, while those along the constriction remain unaffected. Within this constricted region, a parabolic approximation accurately describes the confinement potential, leading to an electron energy spectrum given by

$$E_n = (n + \frac{1}{2})\hbar\omega + \frac{\hbar^2 k_y^2}{2m^*} = \epsilon_n(x) + \frac{\hbar^2 k_y^2}{2m^*}, n = 0, 1, 2, \ldots. \tag{2.14}$$

In each subband $\epsilon_n(x)$, the energy of the electrons varies with position along the y direction through the constriction, with a peak in the exact middle. The constriction passes only those modes satisfying $\epsilon_n(x) \leq E$, with transmission coefficients approaching unity. Electrons in higher energy modes can tunnel through, but most of their amplitude is reflected, allowing only those modes with $\epsilon_n(x) \leq E$ to contribute to the conductivity. With the conductivity for each single mode given by $G = \frac{2e^2}{h}T(\mu)$ from the Landauer formalism described above, the conductivity for N propagating

modes must be

$$G \approx \frac{2e^2}{h} N. \tag{2.14}$$

Therefore the conductance through the QPC is necessarily quantized in units of G_0. This leads to steps in the conductivity as seen in figure 2.3, with the spin degeneracy accounted for by a factor of 2. In the case of Si/SiGe 2DEGs where the partially-lifted valley degeneracy must be included, a factor of 4 is required. Application of a sufficiently large external magnetic field lifts the spin degeneracy and recovers the expected behavior. As the performance of the QPC constriction depends on geometry, temperature, and the presence of nearby defects, deviation from this ideal often occurs, resulting in steps with less pronounced transitions between. [20, 29, 30, 32–34]

2.4 Quantum Dots

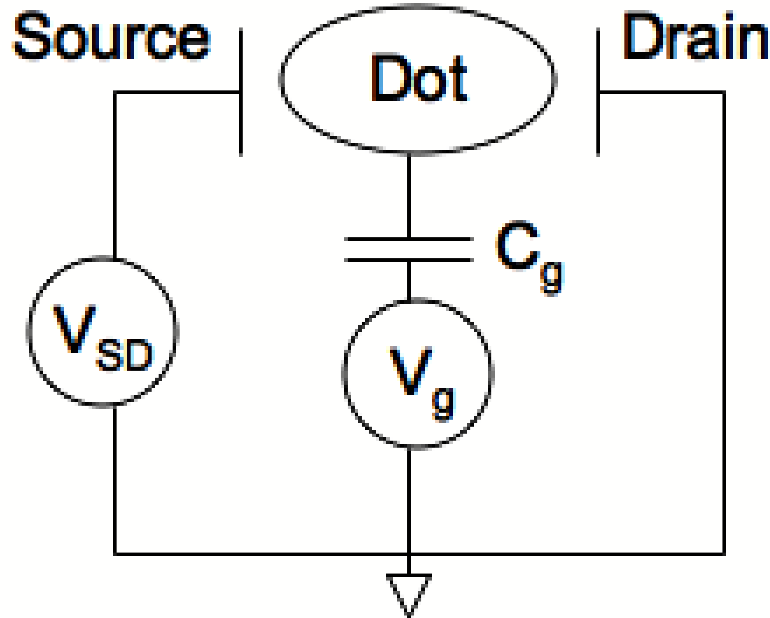


Figure 2.4 Schematic diagram of a quantum dot with weakly coupled source and drain leads.

Quantum dots (QDs) are mesoscopic regions of semiconductors or metals separated by thin potential barriers, often tunnel junctions, that isolate them from nearby source and drain electrodes. In a 2DEG, QDs may be formed by combinations of QPCs that serve as tunable barriers. As QDs may be treated as quasi-zero-dimensional objects when the de Broglie wavelength and the mean free path of electrons on the dot exceed the dimensions of dot, and typical dot may contain as many as thousands to as few as one of these conduction electrons. A very simple model of a QD appears in figure 2.4, with source and drain leads weakly coupled to the dot through controllable tunnel barriers. When the dot is completely decoupled from the leads, the number of electrons on the dot is fixed and quantized by the discrete electronic charge. When the leads become coupled and tunneling occurs, the occupation number of the dot fluctuates. The charging energy E_c is the energy required to add an electron to the dot and is given by the expression

$$E_c = \frac{e^2}{C_\Sigma}, \tag{2.14}$$

where C_Σ is the total self-capacitance of the dot.

Observing the effects of the charging energy requires that certain energy conditions are met. To begin with, the temperature T must be low enough that thermal fluctuations do not overwhelm the charging effects. Thus,

$$k_B T \ll \frac{e^2}{C_\Sigma}, \tag{2.14}$$

where k_B is the Boltzmann constant. In addition to lowering the temperature, lowering the capacitance of the tunnel barriers can help meet this critertion. To a much lesser extent, modifications to the dot geometry can also be used to help meet this first criterion, as the capacitance is also dependent to the dot dimensions, with $C = 8\pi\epsilon_r\epsilon_0 R$ for a disc and $C = 4\pi\epsilon_r\epsilon_0 R$ for a sphere.

Another criterion for observing charging effects arises from quantum mechanics, as the number of electrons on the QD must be well-defined, minimizing the effects of quantum charge fluctuations. This requirement boils down to an uncertainty argument: the energy uncertainty ΔE of the electron

on the dot must be much smaller than E_c to observe charging effects. Taking the time constant $R_t C$ of the tunnel junctions to the dot as the time uncertainty Δt, this criterion derives from the energy-time uncertainty principle $\Delta E \Delta t > h$ as follows:

$$\frac{e^2}{C} R_t C > h \tag{2.14}$$

$$R_t \gg \frac{h}{e^2} = 25.8\text{k}\Omega \tag{2.14}$$

Thus, the resistance of the tunnel barriers to the QD must be much higher than the resistance quantum to observe proper charging effects.

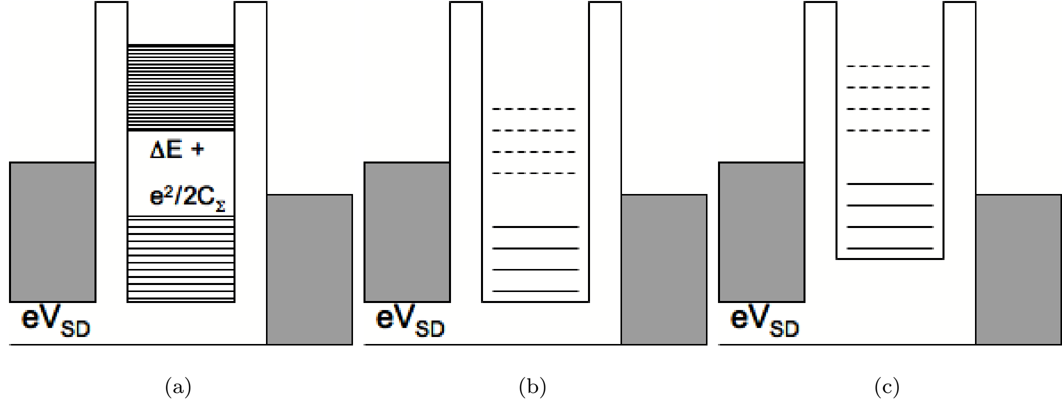
Much as one might expect, electrons tunneling onto and off of the QD causes discrete changes in the potential energy of the dot. Continuous changes in the potential may also be induced by varying the bias potential of a nearby plunger gate V_g capacitively coupled to the QD. Figure 2.5 illustrates the potential landscape of a QD coupled to source and drain leads, with μ_S, μ_{dot}, and μ_D as the chemical potentials of the source, QD, and drain respectively. The source-drain voltage can also be expressed in terms of these chemical potentials as

$$V_{SD} = \frac{\mu_S - \mu_D}{e}. \tag{2.14}$$

Three contributions to the chemical potential of the QD include the single-particle energy levels of electrons on the dot, the charging energy term, and charge induced by the capacitively coupled V_g. This yields the expression

$$\mu_{dot}(N) = E_N + \frac{(N - N_0 - 1/2)e^2}{C_\Sigma} - e\frac{C_g}{C_\Sigma} V_g, \tag{2.14}$$

where N is the occupation number of electrons on the QD and C_g is the capacitance of the coupling between the QD and the plunger gate. Furthermore, given C_S and C_D as the capacitance of the source and drain leads, respectively, the total capacitance is given by $C_\Sigma = C_g + C_S + C_D$. For a given V_g and 0-D energy level spacing of ΔE, the energy required to add one electron to the QD



(a) (b) (c)

Figure 2.5 Schematic diagram of a QD potential under Coulomb blockade (a) and single particle tunneling (b), (c).

can be obtained from the previous equation:

$$\mu_{dot}(N-1) - \mu_{dot}(N) = \Delta E + \frac{e^2}{C_\Sigma}. \tag{2.14}$$

Thus, the addition energy for a single electron is non-zero, allowing for a regime where current cannot flow through the QD due to the available dot energy levels being higher than the Fermi level of the source lead. This regime is known as Coulomb blockade.

Coulomb blockade is lifted when the applied voltage raises the Fermi level of the source, widening the source-drain bias window to include an available dot level. Coulomb blockade (CB) may also be lifted by tuning V_g, adjusting the QD energy levels so that an available one falls within the bias window. For bias small enough that $V_{SD} \leq E_c$ and for $\mu_S > \mu_{dot} > \mu_D$, electrons enter the dot from the source lead, pass through the one available energy level on the QD, and exit via the drain lead, proceeding one at a time in the process of single-electron tunneling. Thus, sweeping V_g in either direction will result in a series of QD energy levels passing through the bias window. Given that current may only pass through these levels, the presence of one in the bias window causes a peak in the conductance through the dot. These conductance peaks are called Coulomb blockade

oscillations (CBO) and occur with periodicity

$$\Delta V_g = \frac{C_\Sigma}{eC_g}(\Delta E + \frac{e^2}{C_\Sigma}). \tag{2.14}$$

Figure 2.6 illustrates the idealized behavior of these oscillations schematically.

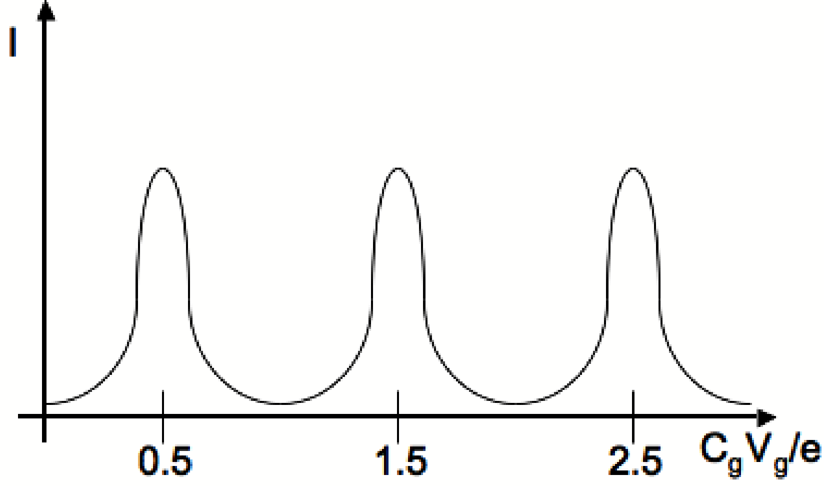


Figure 2.6 Schematic diagram of ideal Coulomb blockade oscillations in an QD.

The shape of the CBO peaks depends on the magnitudes of the three relevant energy scales:

1. For $\frac{e^2}{C_\Sigma} \ll k_B T$, thermal fluctuations dominate and CBO behavior cannot be observed.

2. For $\Delta E \ll k_B T \ll \frac{e^2}{C_\Sigma}$, the classical CB regime is achieved. The effects of the 0-D energy levels are not present, a situation commonly found in metallic QDs and semiconductor quantum dots of larger size.

3. For $k_B T \ll \Delta E \ll \frac{e^2}{C_\Sigma}$, the quantum CB regime is achieved and the single particle levels due to size quantization become involved in transport through the QD.

Orthodox CB theory describes the case of classical CB, with the CBO peaks defined by

$$\frac{G}{G_\infty} = \frac{1}{2}\cosh^{-2}\left(\frac{\delta}{2.5k_B T}\right), \tag{2.14}$$

with $\delta = e(C_g/C_\Sigma)|V_{g,res} - V_g|^2$ where $V_{g,res}$ is the gate voltage corresponding to the conductance peak location. The temperature dependance of the peak shape is apparent, although the maximum peak height is independent of temperature and equal to half the high temperature limit G_∞. At low temperatures, the electron one the dot must tunnel out to the drain first before another may tunnel on from the source, reducing the conductance by a factor of 2. Additionally, thermal fluctuations overwhelm CBO behavior when $k_B T > 0.3e^2/C_\Sigma$.

A proper description of the quantum CB regime must include a temperature dependence in the height of the conductance peaks, with a maximum of almost $0.75G_\infty$, rather than the classical limit of $0.5G_\infty$. Thus, the conductance of a single peak in quantum CB theory is given by

$$\frac{G}{G_\infty} = \frac{\Delta E}{4k_B T} \cosh^{-2}\left(\frac{\delta}{2k_B T}\right). \tag{2.14}$$

In both the classical and quantum CB regimes, the current through the QD exhibits strong dependence on potential of the capacitively coupled gate electrode. This is analogous to the dependence of the current flow in a field-effect transistor on the voltage of the gate, leading to the other common name for quantum dots: the single electron transistor (SET). [35–39]

2.5 The Radio-Frequency Superconducting SET as a Charge Sensor

A important variation on the SET occurs in the case of a superconducting metallic island QD designed to operate as an ultrafast and ultrasensitive charge sensor. Current RF-SET methods have achieved charge sensitivities approaching the shot-noise quantum limit of $1.6 \times 10^{-6} e/\sqrt{\text{Hz}}$ and routinely achieve sensitivities $< 10^{-5} e/\sqrt{\text{Hz}}$, corresponding to a charge fluctuation of $10^{-5}e$ being detected over the time scale of 1 second or a charge fluctuation of e being detected over the time scale of 10 μs. By embedding the SET serving as a detector in a tank circuit with a resonant

frequency in the RF and capacitively coupling the RF-SET to a nearby nanostructure, such as a QD formed in a buried 2DEG, charge fluctuations of the QD system cause detectable changes in the properties of the RF-SET. The specifics of this implementation are discussed in more detail in this final section of chapter 2.

In the case of a normal-state SET capacitively coupled as a charge detector, charge fluctuations in the surrounding environment causes the the chemical potential of the SET to shift in response, producing changes in the current through the SET island. This implementation results in very small changes in current occurring at rather fast rates, a signal that is very difficult to detect. In the case of the RF-SET as seen in figure 2.7, the SET becomes part of a resonant LCR circuit whose reflected power at the resonant frequency depends strongly on the differential resistance R_d of the RF-SET. Taking advantage of a superconducting RF-SET allows further reduction of the tunneling resistance, improving the strength of the signal modulation at resonance. Additionally, operating the RF-SET at higher frequencies avoids the effects of the $1/f$ background charge fluctuation noise that dominates low-frequency measurements of small signals.

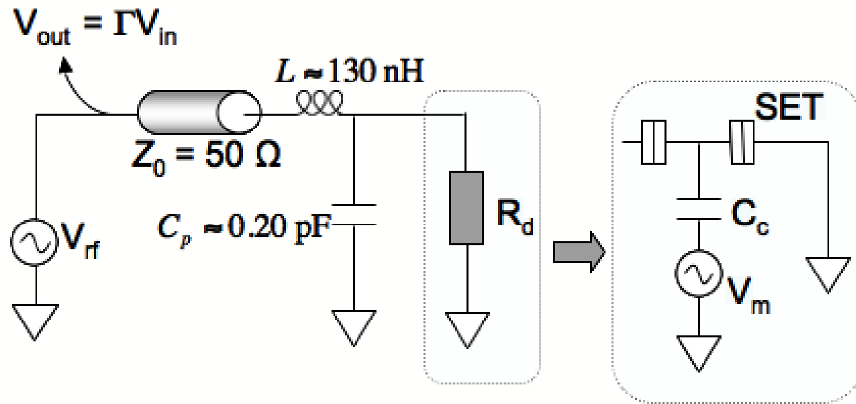


Figure 2.7 Schematic of an SET embedded in an RLC tank circuit functioning as a charge detector.

From the schematic in figure 2.7, the impedance looking into the tank circuit is

$$Z = i\omega L + \frac{1}{i\omega C} = \frac{R_d}{1+\omega^2 C^2 R_d^2} + i\frac{\omega L - \omega C R_d(1-\omega^2 CL)R_d}{1+\omega^2 C^2 R_d^2}. \tag{2.14}$$

This expression simplifies for the on-resonance case, as the imaginary term shrinks to zero, yielding

$$\frac{\omega L - \omega C R_d(1-\omega^2 CL)R_d}{1+\omega^2 C^2 R_d^2} = 0, \tag{2.14}$$

providing a relation that gives the resonance frequency

$$\omega_0 = \sqrt{\frac{1}{LC}}\sqrt{1-\frac{L/C}{R_d^2}}. \tag{2.14}$$

At resonance, combining this with the prior expression for the impedance reduces it to

$$Z = \frac{L}{CR_d}. \tag{2.14}$$

Since operating the RF-SET involves measuring the reflected power of the tank circuit, the dependence of reflection coefficient Γ on the impedance Z of the tank circuit is required. As Γ is defined as the ratio of the incoming and outgoing voltage waves V_{in} and V_{out}, the following expression obtains:

$$\Gamma = \frac{V_{out}}{V_{in}} = \frac{Z-Z_0}{Z+Z_0} = -1 + \frac{2Z}{Z+Z_0}, \tag{2.14}$$

with $Z_0 = 50\Omega$ representing the characteristic impedance of the coaxial RF transmission line. Applying the simple expression for Z provides a dependence on R_d

$$\Gamma = -1 + \frac{2}{1+Q_0^2(Z_0/R_d)} Q_0^2 \frac{Z_0}{R_d}, \tag{2.14}$$

where the unloaded quality factor $Q_0 = \sqrt{\frac{1}{C_p}\frac{1}{Z_0}}$. Perfect impedance matching occurs when $R_d = Z_0/Q_0^2$ and results in $\Gamma = 0$. For the limiting case of $R_d \to \infty$ and $\Gamma \to -1$, all the input power is completely reflected, as one should expect from a tank circuit with infinite input impedance. The unloaded quality factor Q_0 factors into the bandwidth at resonance $B = f_0/Q_0$ and the amplitude of the RF signal that actually reaches the SET $V_{SET} = 2Q_0 V_{in}$.

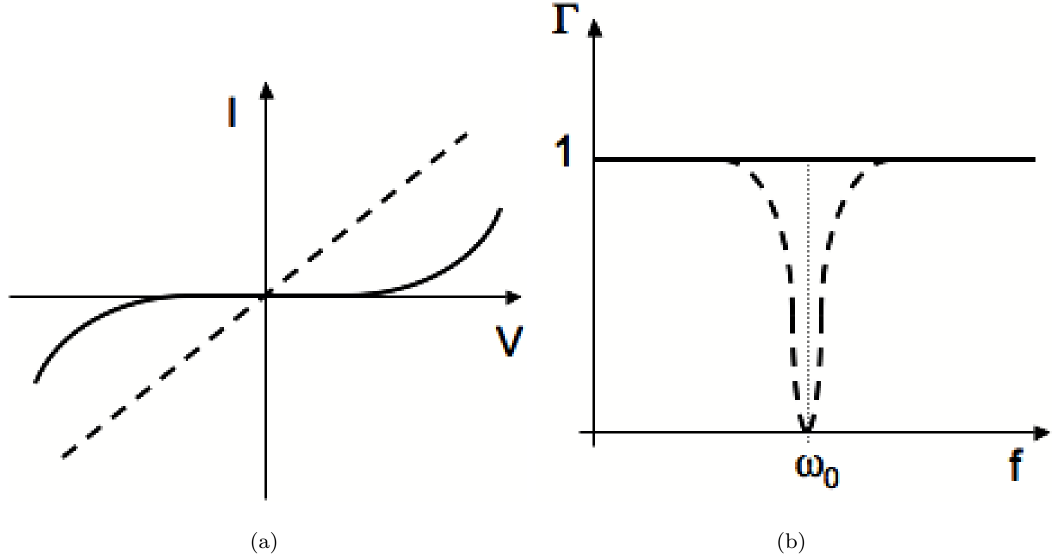


Figure 2.8 Cartoon of RF-SET performance illustrating hypothetical $I - V$ (a) and reflected coefficient (b) curves for in (solid) and out (dashed) of Coulomb blockade.

By tuning the RF-SET to an operating point where the charge fluctuations of the coupled QD can drive the SET in and out of Coulomb blockade (CB), the RF-SET can serve as a charge detector whose bandwidth is limited by impedance matching of the resonant tank circuit. Figure 2.8 illustrates the DC and RF performance of an SET both in and out of CB. Consistent with the preceding theory, the SET exhibits a differential resistance R_d, taken as the inverse of the slope of the $I - V$ curve, of nearly infinity when under CB and under small source-drain bias conditions. Alternatively, when the RF-SET is out of CB, near-perfect impedance matching may be achieved, resulting in $\Gamma = 0$. The CB modulation in Γ represents changes in the reflected voltage that are larger and easier to detect than the tiny current fluctuations caused by the change in the charge state of the coupled QD. [1, 13, 13–15, 40–44]

Chapter 3

Experimental Methods

Fabricating and measuring mesoscopic devices like quantum dots and RF-SETs requires a host of highly specialized techniques. This chapter presents the details of these methods, with specific emphasis on how they apply to this work. A step-by-step list of the complete device fabrication sequence appears in Appendix A at the end of this document as a convenient summary.

3.1 Device Patterning

This section details the two main methods of patterning devices: photolithography, with resolution of $\sim 2\mu$m with the typical academic research apparatus, and electron beam lithography, with resolution of a few tens of nanometers.

3.1.1 Photolithography

The process of photolithography remains essential to the semiconductor industry, making it an economically important technology. As a consequence of this, a wide array of photolithographic processes exist, such that applying one suitable to the experiment at hand is usually quite straight-

forward. In general, photolithography involves fives general steps: coating the substrate with photoresist, exposing the resist to UV radiation through a mask, developing the pattern, depositing or removing material, and lifting off the resist. These steps are depicted in figure 3.1 below.

Preparing the substrate material, pieces of SiGe heterostructure material in the case of this work, to receive photoresist involves cutting it to the right size and cleaning it. Using a ruler and a diamond-tipped scribe, one can cut SiGe wafer into chips of the desired size, usually pieces approximately 4x6 mm in area. After marking and scoring the polished top surface of the wafer, one can invert the material and apply pressure on the back side of the score mark, resulting in the sample chip cleaving from the wafer in a controllable fashion. Unlike the sharp cleaving along crystal planes typically seen in GaAs samples, the edges of Si and SiGe samples routinely exhibit uneven sloping edges that make subsequent handling with tweezers more difficult; extra care must be taken to avoid destroying devices on the surface with errant tweezer tips. Once cleaved, immerse the bare sample in a bath of acetone and placed in a sonicator, an ultrasonic cleaner, for at least 10 minutes to remove any residues and dust that may have accumulated through storage, handling, or cleaving. After sonication, rinse sample in isopropanol (IPA) for 3-5 seconds, followed by blowing dry with pure dry nitrogen gas.

With clean samples in hand, the remainder of the photolithography process occurs in the cleanroom environment, where the lighting is filtered to prevent premature exposure of the ultraviolet-sensitive photoresist to ultraviolet (UV) radiation. The first step in the cleanroom involves coating the sample with photoresist, a polymer engineered to change its structure after exposure to UV radiation. In the case of positive resist, the cross-linking bonds break down in the presence of UV light, softening the material and making it susceptible to removal with the right developer solution. Negative resist works in reverse, hardening under irradiation. Fabrication of the devices described in this work used exclusively positive resist, specifically Shipley 1813 resist. [45]

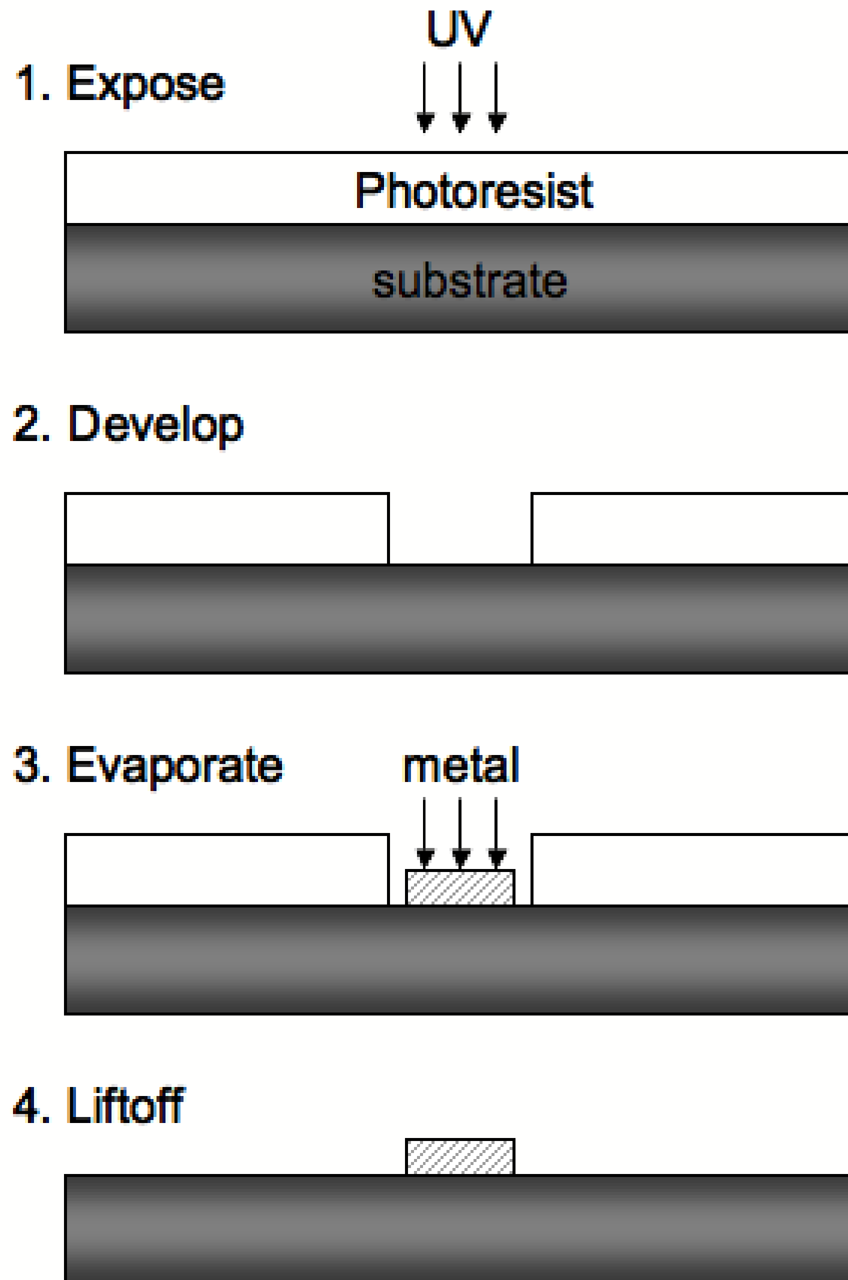


Figure 3.1 Schematic diagram of the photolithography process.

To actually coat a sample, affix it to the removable stage (or "puck") from the spin-coater using double-sided carbon tape. Be sure to position the sample off-center, closer to the edge of the puck, so that the resist piles up as an edge-bead along only one side of the sample, rather than at all four corners as it would if the sample is positioned in the exact center. Having an edge-bead limited to one side makes subsequent alignment to the photomask easier. Using a pipette, apply enough photoresist to completely cover the sample and spill over the edges. Spin for 5 seconds at 500 rpm, followed by 45 seconds at 4000 rpm. Bake the sample on a hotplate for 2 minutes at 90°C to evaporate solvent and form cross-linking bonds in the resist polymer. This results in a resist coating approximately 1.25 μm thick. [45]

Load sample and appropriate photomask into the mask aligner. The aligner instrument allows for accurate registration of the photomask to the sample, with precisions better than 2 μm in the hands of an experienced user. Adjust microscope to bring correct section of mask pattern into focus. Slowly raise sample stage until sample barely comes into focus, allowing room to adjust stage position to align pattern to sample. Once aligned, raise sample into firm contact with the mask and expose to UV source for 14 seconds. After exposure, develop pattern by immersion in Microposit MF-321 developer, a metal-free organic base solution of (2.3% by mass) tetramethyl ammonium hydroxide $(CH_3)_4NOH$ in water, for 45 seconds, followed by 3-5 seconds rinse in deionized water. Blow sample dry with pure dry nitrogen gas. Developing the pattern completes the cleanroom portion of photolithography; etching or metallization follows, depending on the step. After further processing, finish the photolithography process by placing sample in covered acetone bath for at least 1.5 hours to dissolve and liftoff remaining photoresist. To complete liftoff, sonicate in same acetone bath for 3-5 seconds, rinse for 3-5 seconds in IPA, and blow dry with pure dry nitrogen gas.

3.1.2 Electron Beam Lithography

This section describes the process of electron beam (e-beam) lithography using a scanning electron microscope (SEM). Much of the process parallels that of photolithography, as e-beam lithography also involves fives general steps: coating the substrate with photoresist, exposing the resist to the electron beam according to a computer-controlled pattern, developing the pattern, depositing or removing material, and lifting off the resist. These steps are depicted in figure 3.2 below.

Prepare sample for e-beam lithography by ensuring its cleanliness, either by continuing processing with a sample cleaned at the end of prior steps or by preparing new chips following the procedure described in the third paragraph of the previous subsection on photolithography. Once clean, to facilitate easier handling, affix sample to 1 cm square brass plate after spin-coating brass plate with old e-beam resist for 10 seconds at 1000 rpm. Bake on hotplate for 3-5 minutes at 90°C. Follow this with a two-layer e-beam resist coating. First, spin-coat sample with PMMA-495K (polymethylmethacrylate, 495,000 dalton average molecular weight, a positive e-beam resist) e-beam resist at 4000 rpm for 30 seconds and bake for 5-10 minutes at 180°C. Spin-coat sample with PMMA-950K (also PMMA, but with 950,000 dalton average molecular weight) e-beam resist at 4000 rpm for 30 seconds and bake for 5-10 minutes at 180°C. This recipe yields resist films with a total thickness of 200 nm or less. [1, 12, 15]

This two-layer resist takes advantage of the relative susceptibilities of the different weight polymers to e-beam irradiation. The larger weight molecules represent longer individual chains with more cross-linking, making the polymer more robust under irradiation. As a result, the lower layer of resist, the "softer" PMMA-495K, exhibits an undercut with respect to the upper layer of PMMA-950K after exposure and developing. The overhanging mask of PMMA-950K actually defines the pattern for subsequent metallization, while the undercut allows for cleaner liftoff. Pre-exposing the lower layer of resist to UV radiation results in enhanced undercutting, a feature utilized to great

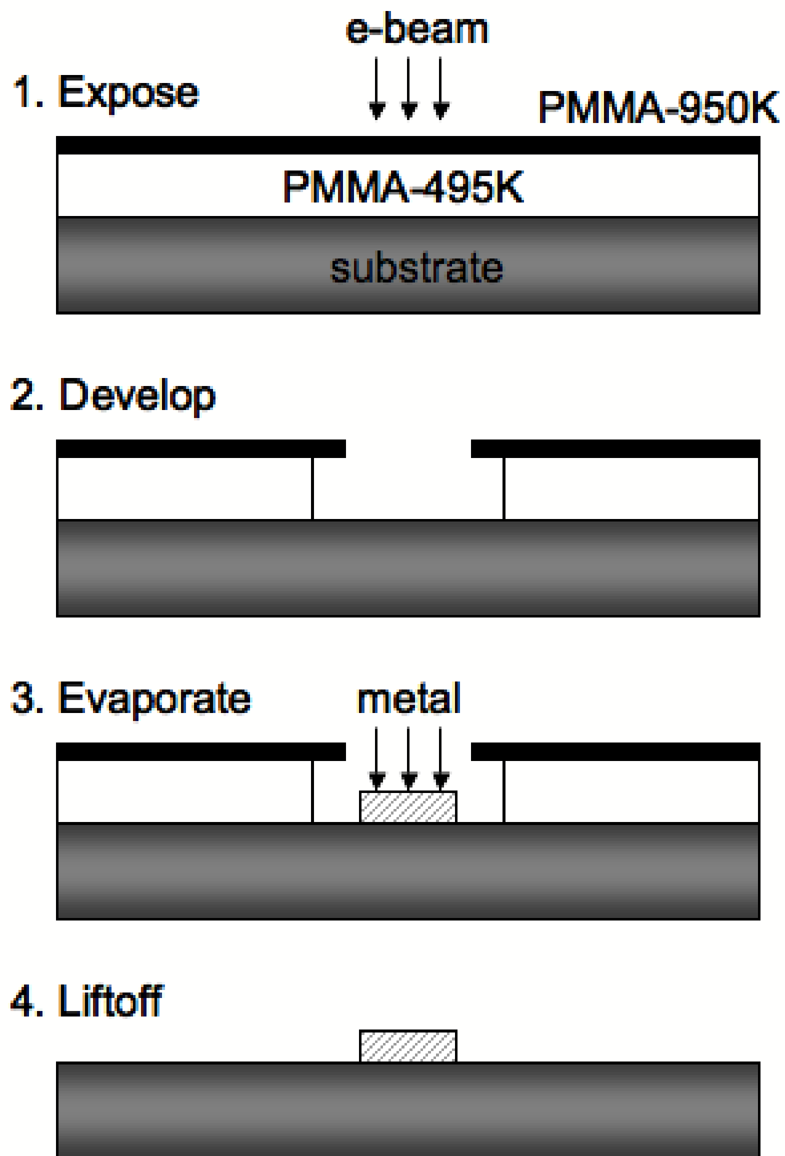


Figure 3.2 Schematic diagram of the e-beam lithography process.

effect in the process of shadow evaporation, described later in this chapter. [1,12,15]

Exposing the device pattern on the SEM requires proper adjustment of the microscope and computer control of the e-beam during exposure according to a prescribed pattern defined by user-generated computer-aided design (CAD) files. A schematic depicting this arrangement appears in Figure 3.3 below. Using proprietary software, the Nanometer Pattern Generation System developed by Joe Nabity, pattern files drawn in a CAD environment are assigned exposure doses in terms of charge per unit area or length, depending on the type of pattern, by a run file that allows the NPGS program to control the scanning of the e-beam. A combination of prior experience and trail-and-error determines the best dose values for the different features of a pattern. The NPGS program also provides a precision alignment capability that allows for registration of 20-30 nm between different exposures. [1,12,15]

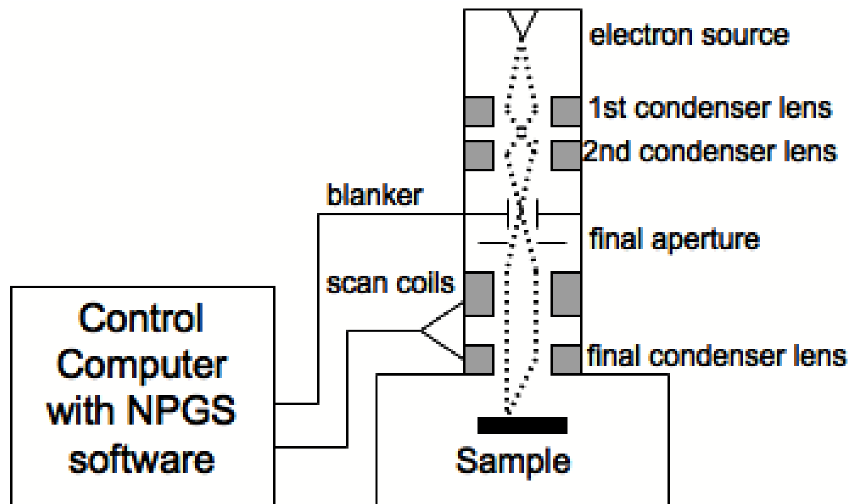


Figure 3.3 Schematic diagram of the SEM apparatus for e-beam lithography.

After exposure on the SEM, develop the pattern by immersing sample in MIBK/IPA mixture (methylisobutyleketone, also known as 4-methyl-2-pentanone, 3:1 ratio by volume) for 60 seconds, followed by 40 seconds immersion in pure IPA, finishing by blowing dry with pure dry nitrogen. The

strongly polarized ketone functional group on the MIBK molecule dissolves the resist weakened by e-beam exposure, in a milder version (due to the lower polarity of MIBK) of the liftoff process that occurs as a result of the ketone group in the acetone molecule. The developing process exhibits some temperature dependence, so that developing samples at the same temperature each time yields more consistent results. Additionally, since the smallest features are the most sensitive to variations in beam current, resist film quality, and temperature of the developing solution, arrays of patterns on scrap wafer material with slight variations in the dosing are used to pinpoint the best recipe before committing to real device fabrication. [1, 12, 15]

Once developed, a patterned mask of e-beam resist remains on the surface of the sample. Further processing, either material removal or deposition may then be applied to the exposed area of the sample surface. After this further processing, finish the lithography process by placing sample in covered acetone bath for at least 6 hours (preferably longer) to dissolve and liftoff remaining e-beam resist. To complete liftoff, sonicate in same acetone bath for 3-5 seconds, rinse for 3-5 seconds in IPA, and blow dry with pure dry nitrogen gas. [1, 12, 15]

3.2 Material Growth and Deposition

This section extends the discussion of methods to include the details of the Si/SiGe heterostructure growth, as well as the various methods of deposition by vacuum evaporation and the general process for annealing ohmic contacts.

3.2.1 Si/SiGe Heterostructure

As detailed in chapter 2, the methods of ultra-high vacuum chemical vapor deposition (UHVCVD) were used to grow the Si/SiGe heterostructures used in these experiments. The strained Si quantum well containing the 2DEG exists atop a strain-relaxed $Si_{0.7}Ge_0.3$ buffer layer that itself sits atop

Table 3.1 Si/SiGe heterostructure material grown at University of Wisconsin - Madison

Batch Number	n (cm^{-2}	μ(cm^2/s)
070522	7.35×10^{11}	7777
070628	5.5×10^{11}	22500
070824	5.5×10^{11}	22500
08011201	N/A	N/A
08031201	N/A	N/A

strained $Si_{1-x}Ge_x$ layers descending in Ge concentration from $x = 0.3$ down to the pure n-type Si wafer substrate at the bottom. Above the 2DEG, another strain-relaxed $Si_{0.7}Ge_0.3$ layer is grown, capped by a thin layer of Si. The width of the quantum well is 80 angstroms and lies at a depth of 60–80 nm beneath the surface of the wafer, depending on the batch of material. Further details on the growth of these materials can be found in references [17, 20–23, 25, 28], and the details of those batches used for this work appear in the table below. While carrier density and mobility data are not available for the final two batches, they were grown according to the same recipe as batch #070824, implying that they will have similar properties. Additionally, figure 3.4 below illustrates the layers of the Si/SiGe heterostructure.

3.2.2 Thermal Evaporation

In general, thermal evaporation involves heating a source material in a high vacuum environment, so that the material vaporizes upon melting and coats anything in the chamber exposed to the source. A wide variety of metals evaporate easily with thermal sources, which involve direct heating by passing a high current through a resistive source heater, typically refractory elements such as Mo, Ta, or W, to melt the metal inside. Some metals prove more difficult due to sublimation, as in

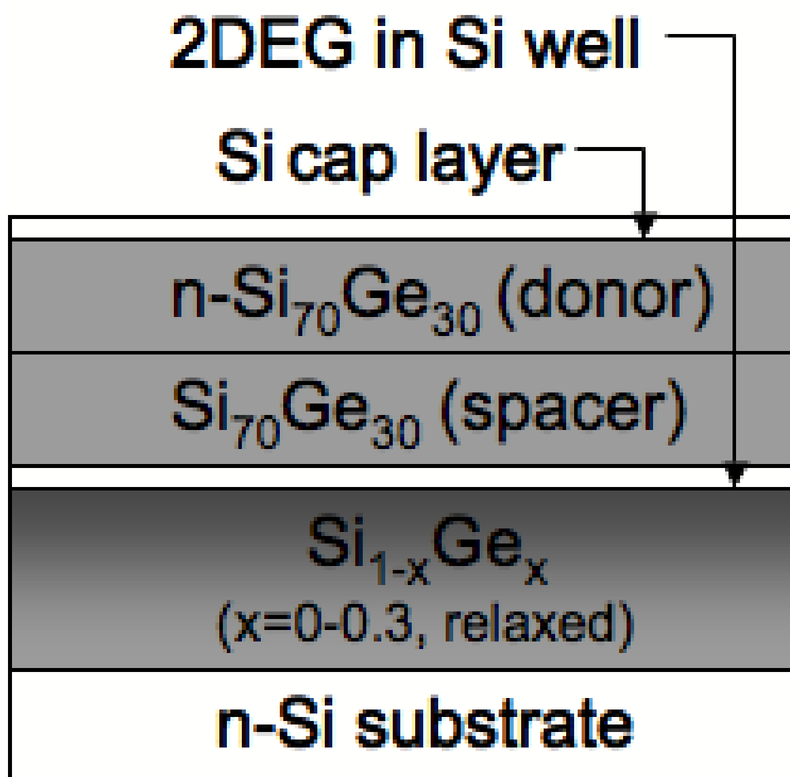


Figure 3.4 Simplified schematic of the Si/SiGe heterostructure.

the cases of Cr and Sb, or as a result of alloying with the refractory metals in the source heaters, as in the cases of Pd and Ni. Controllable evaporation of these metals requires different types of heaters that the standard filament basket or "boat", a broad flat piece of refractory metal with a recessed dimple for holding the source metal. Certain insulators can also be thermally evaporated, although these require additional preparations involving the type of resistive source used and careful attention to the current applied during heating. [46] For the purposes of this work, the thermal evaporator was used exclusively for the deposition of metals, primarily in the case of the ohmic contact metallization.

Figure 3.5 above depicts a schematic of a generalized thermal evaporator. The basic procedure for operation involves several steps. First, after checking to make sure the high vacuum valve is closed, vent the vacuum chamber to load the sample and appropriate source(s). Multiple sources are commonplace: the Rimberg laboratory has two custom-rebuilt thermal evaporators, one with two available sources and another with three. Begin pumping out by closing the backing valve and opening the rotary vane mechanical roughing pump to the main chamber. Meanwhile, fill the cold trap with liquid nitrogen to facilitate efficient operation of the high vacuum diffusion pump. Once the pressure inside the main chamber drops below 100 mTorr, close the roughing valve and open the backing valve again. Follow this by slowly opening the high vacuum valve to allow the diffusion pump access to the main chamber, checking to make sure the backing pressure remains at ~100 mTorr or less. Once the high vacuum valve is completely open, turn on the ion gauge to monitor the chamber pressure. Wait for the pressure to reach at least $\sim 2\times10^{-6}$ Torr, refilling the cold trap with liquid nitrogen as necessary. Note that higher deposited film quality is achieved at lower pressures. When the desired pressure is reached, turn on the deposition monitor, tune it to the correct materials parameters, and proceed with evaporation of the source material(s), slowly ramping up the current on each one in turn to achieve the desired deposition rate. After completing the evaporation, close

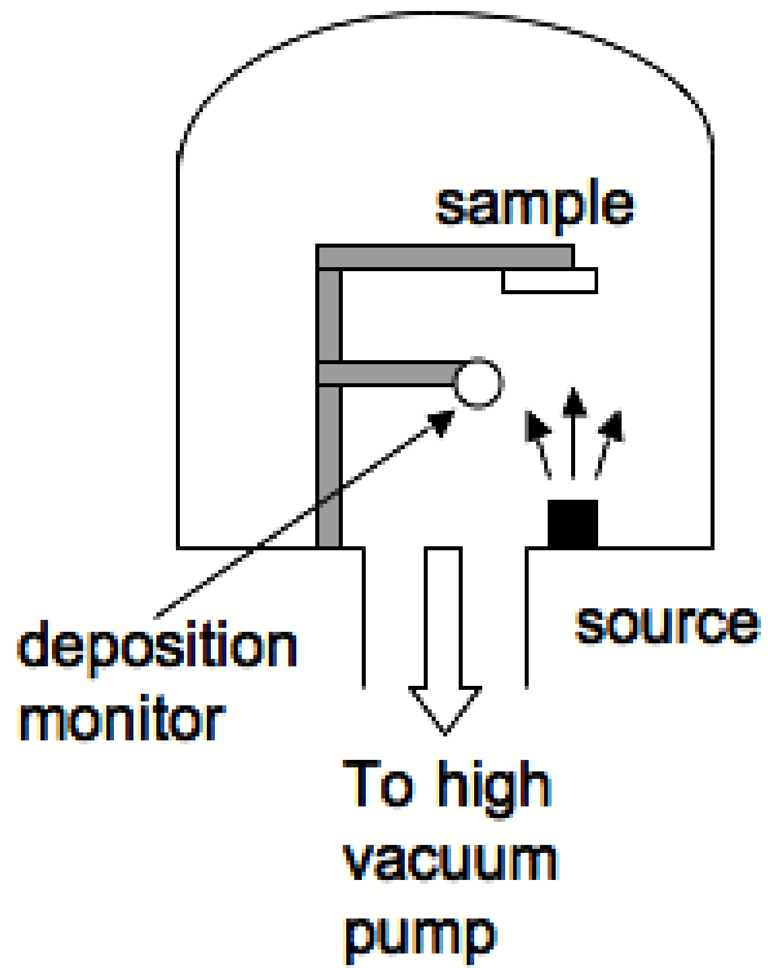


Figure 3.5 Schematic diagram of a thermal evaporator.

the high vacuum valve, and wait a few minutes for the source heaters to cool down before venting. After removing the sample, rough out the chamber again by closing the backing valve, opening the roughing valve, waiting for the chamber to pump down to 300-400 mTorr, closing the roughing valve, and finally reopening the backing valve to leave the evaporator in standby mode. Place sample in covered acetone liftoff for 1.5 (for photoresist) to 6+ (for e-beam resist) hours. To complete liftoff, sonicate in same acetone bath for 3-5 seconds, rinse for 3-5 seconds in IPA, and blow dry with pure dry nitrogen gas. [1, 12, 15]

3.2.3 Electron Beam Evaporation

Much like the thermal evaporator, the e-beam evaporator heats sources in a high vacuum environment to produce vapors that coat objects in the vacuum chamber. A few key differences in the physics driving these two processes make the e-beam evaporator a better choice for depositing many materials, particularly insulators. The major difference lies in how the source materials are heated: an e-beam evaporator exposes the source material to a beam of electrons that directly heats it by irradiation, unlike the thermal evaporator where the sources are melted by conduction from a resistive heater. [46–48] Since the vacuum pumping apparatus for the e-beam evaporator, a high vacuum turbomolecular pump backed by a rotary vane roughing pump, is very similar to that of the thermal evaporator, Figure 3.6 below only depicts the source apparatus inside the vacuum chamber, including the electron gun and the crucible containing the source material.

E-beam evaporations can be performed by following the procedure outlined here. As the vacuum pumps are typically off, one must first start the pumping system, allowing the turbopump about 15 minutes to spin up to speed. Meanwhile, vent the chamber and load the sample as well as the source materials. The Edwards AUTO 500 Coater system can accommodate up to 4 different sources in a rotating turret of copper hearths. Each source material will evaporate most efficiently when the

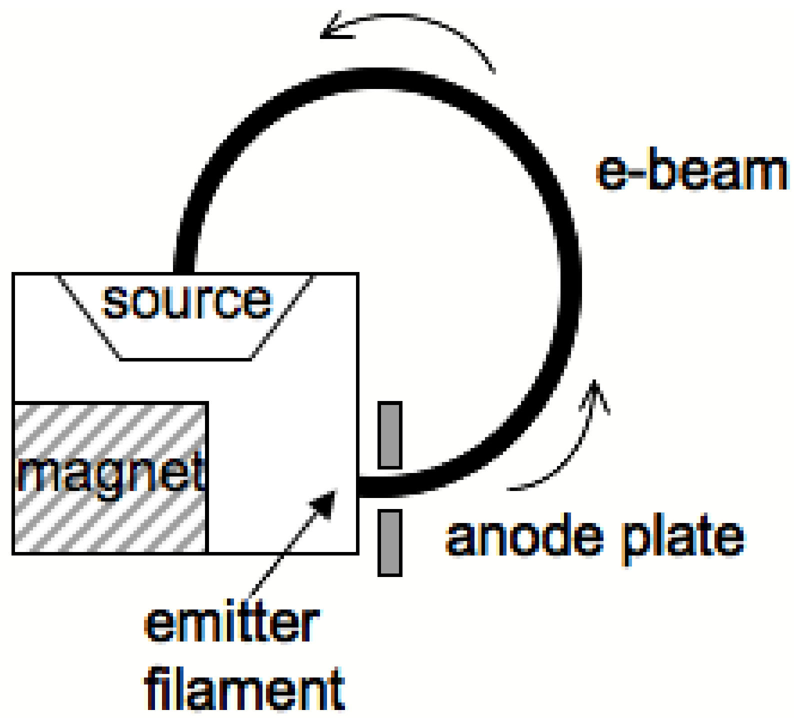


Figure 3.6 Schematic diagram of the source apparatus from the e-beam evaporator.

Table 3.2 E-beam Evaporation Crucible Guide

Source Material	Au	Sb	Ti	Pd	SiO_2
Crucible Material	Vitreous carbon	Intermetallic	Graphite	Graphite	No Crucible

hearth is prepared with the correct crucible or lack thereof. Table 3.2 indicates the crucible type used for each of the materials evaporated with the e-beam evaporator as a part of this work. [46–48]

Once the sample and sources are loaded into the chamber and the pumps are up to speed, evacuate the chamber and wait for the pressure to reach $\sim 5\times10^{-6}$ Torr. Proceed with evaporation by rotating source turret to appropriate material, setting the deposition monitor to the correct parameters for the material being deposited, and turning on the electron gun. Once the accelerating voltage for the e-beam has stabilized, slowly ramp up the beam current until the chamber pressure begins to increase, indicating outgassing and the start of the melting of the source material. In many cases, using the sweep controls to raster the beam across the surface of the crucible yields more efficient evaporation. Achieve the desired rate of deposition and open the shutter to allow material to coat the sample. Switch between multiple sources as necessary, ramping down the beam current before switching. Complete the evaporation process once final source has cooled by sealing chamber and venting to atmosphere. Remove sample and source(s) and rough out chamber to 100-200 mTorr before sealing and stopping the pumps. [47, 48] Place sample in covered acetone liftoff for 1.5 (for photoresist) to 6+ (for e-beam resist) hours. To complete liftoff, sonicate in same acetone bath for 3-5 seconds, rinse for 3-5 seconds in IPA, and blow dry with pure dry nitrogen gas.

3.2.4 Shadow Evaporation

A specialized form of evaporation, shadow evaporation involves the use of multiple sources and tilting the sample to achieve more complicated device designs with just one lithography step. Shadow

evaporation represents the primary method for fabricating RF-SET devices out of Al/AlO_x films. In the Rimberg lab, only the thermal evaporators have the tilting stages needed for shadow evaporation, although it could also be performed in an e-beam evaporator with the requisite tilting stage. In addition to tilting the sample and switching sources between deposition layers, shadow evaporation also demands extra sample preparation in the early stages to enhance the undercut in the lower layer of e-beam resist. During process of coating the sample with e-beam resist, an extra layer of PMMA-495K must be applied, using the same spinning and baking parameters as the first one. This is followed by a 10-minute pre-exposure of the PMMA-495K layers to soften these bottom layers of resist, further enhancing the undercut. Figure 3.7 below illustrates the steps of shadow evaporation.

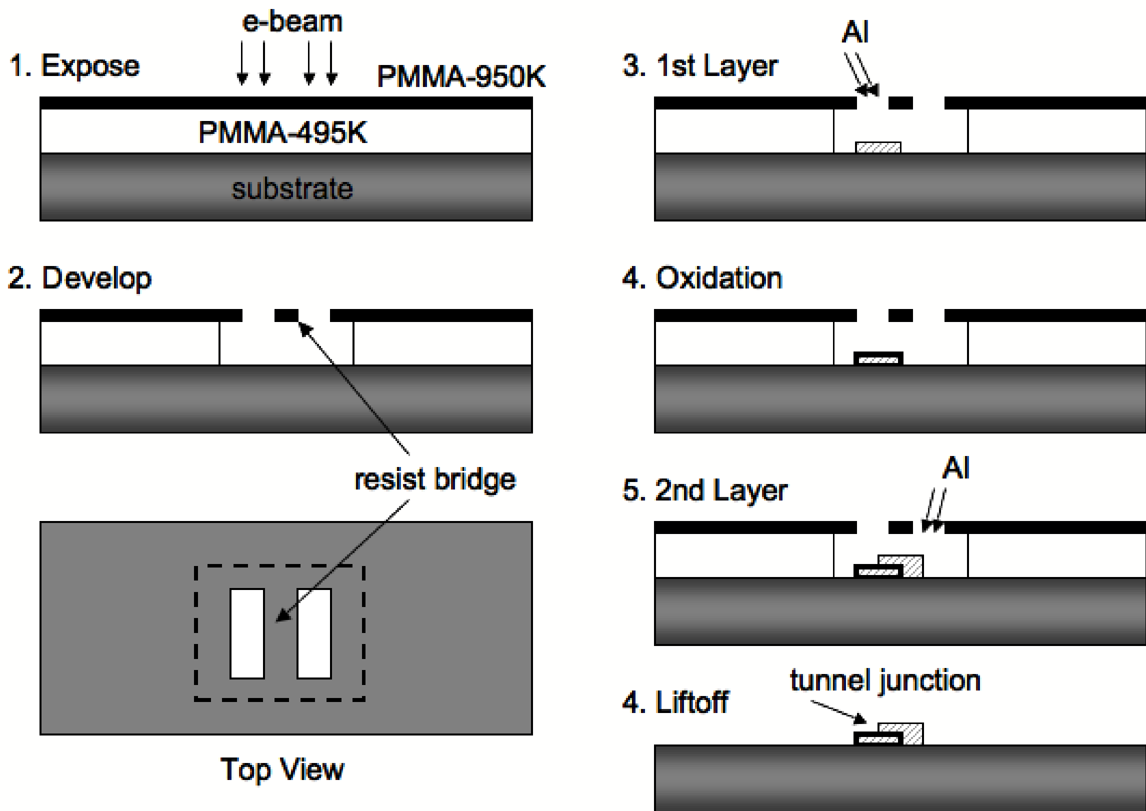


Figure 3.7 Schematic diagram of the shadow evaporation process.

The specific process for fabricating RF-SETs uses the two-source thermal evaporator. To begin, place sample on the stage as usual, also loading Al metal in both sources (5 pellets in source A, 6 pellets in source B). Proceed with the normal pumpdown procedure, but wait until the chamber pressure reaches into the upper 10^{-7} Torr range, since higher quality films are preferred in the case of the superconducting RF-SET. After tilting the stage pointing down to the left, traversing approximately 11.5 turns on the tilt adjustment knob from the centered position, evaporate from source A, depositing 20 nm Al for the first layer. Then, form aluminum oxide for the tunnel junctions by allowing 100-110 mTorr of O_2 mixture into chamber for 3 minutes after sealing the high vacuum valve. Note that oxidation recipes are known to vary quite a bit, as the pressure and time conditions used are not sufficient to completely passivate the surface of the Al film; thus the growth rate of the aluminum oxide depends on factors not under rigid experimental control. [1,12,15]

After the proper time has elapsed, pump out the oxygen and tilt sample back the other direction, pointing down to the right, traversing a total of 22-23 turns between layers. This amount of tilt results in a shadow overlap of about 120-150 nm when using a doubly-thick bottom layer of PMMA-495K resist. After tilting, deposit 40 nm Al for the second layer. In this way, the requisite superconductor-insulator-superconductor junctions are created that form the RF-SET. Remove sample, rough out chamber, and leave evaporator in standby mode, following the same procedure as described above for a normal thermal evaporation. Place sample in covered acetone liftoff for at least 6 hours (preferably longer). To complete liftoff, sonicate in same acetone bath for 3-5 seconds, rinse for 3-5 seconds in IPA, and blow dry with pure dry nitrogen gas. [1,12,15]

3.2.5 Ohmic Contact Growth

A more thorough discussion of the diffusion and alloying processes at work during ohmic contact growth will appear in chapter 4; this subsection simply details the steps used to fabricate ohmic

contacts, specifically for the recipe that eventually proved best. In general, ohmic contacts to the 2DEG are formed by depositing metal on the surface and annealing the sample to alloy the metal on the surface to alloy and/or diffuse into the semiconductor material deep enough to provide a conducting pathway to the buried 2DEG.

In the case of SiGe, the deposited metal does not penetrate the native SiO_2 on the surface, so this must be removed first. Since this native oxide will begin reforming immediately, albeit slowly at room temperature, one should prepare the thermal evaporator in advance by pre-loading source materials: Au, Sb, and Au, for the recipe ultimately decided to work best for SiGe devices. To remove the native oxide, dip sample in buffered oxide etch solution (BOE, a diluted aqueous mixture of HF and NH_4OH, available as pre-mixed industry standard reagent) for at least 15 seconds. As quickly as possible ($<$ 2 minutes), load sample into thermal evaporator and immediately begin pumpdown. When pressure reaches $\sim 5\times10^{-6}$ Torr, proceed with evaporation, depositing first 10 nm Au, then 1-2 nm Sb, followed by 70 nm Au. Complete evaporation and place sample in covered acetone liftoff for at least 1.5 hours. To complete liftoff, sonicate in same acetone bath for 3-5 seconds, rinse for 3-5 seconds in IPA, and blow dry with pure dry nitrogen gas.

Ohmic contact annealing uses the strip heater. Begin by loading sample into strip heater and flushing chamber for 3-5 minutes with a reducing gas mixture (20 percent H_2, balance of nonreactive gas, usually He, Ar, or N_2). The reducing gas prevents oxide formation at the surface by reacting with oxygen on the surface to form water vapor that is flushed away by the gas flow. Anneal for 1 minute at 110°C to allow remove any adsorbed water, followed by 4 minutes at 410°C to grow the ohmic contacts. Figures in chapter 4 depict the results ohmic contact growth, as well as presenting micrographs of the ohmic contact surface to illustrate the phase transition.

When encountering a new batch of material for the first time, double-checking the ohmic contact recipe for success is often a wise idea. In the case of most materials, the ohmic contacts can be

easily checked at room temperature with a probe station. In the case of SiGe, the abundance of thermally-activated free carriers at room temperature requires that the sample be connected to a dunker apparatus that allows electronic measurements of the sample while immersed in a cryogenic bath. Since these thermally-activated carriers in SiGe tend to freeze out when $T \sim 10$ K, the sample must be immersed in liquid helium ($T = 4.2$ K) to confirm the ohmic contact functionality.

3.3 Material Removal

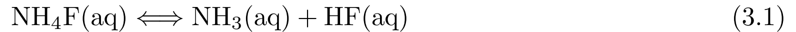
This section details the etching methods used in this work to controllably remove material during device fabrication, including both wet and dry processes, as well as some discussion of their relative merits.

3.3.1 Wet Etching

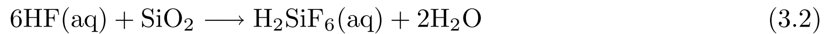
Wet etching involves immersing the sample in a chemical solution tailored to remove the exposed sample material in a controlled and predicable way. Wet etching usually involves a two-fold process: oxidation of the substrate, and oxide removal, with both reactions typically occurring simultaneously as the etch proceeds. Additionally, the typical wet etch removes material isotropically, so that the exposed pattern is widened as much as it is etched into the substrate. Given that the chemistry can be specifically designed to etch only certain materials, the wet etch has the advantage of high selectivity. Wet etching also has the advantage of being more "gentle" to the device than an energetically-driven process like the reactive ion etching detailed in the next subsection, as wet etches are routinely designed to work at close to ambient temperature conditions.

The buffered oxide etch (BOE) used in conjunction with the ohmic contact formation represents an industrially standardized way to selectively remove SiO_2 without penetrating the underlying Si or SiGe. The BOE reagent is readily available in a variety of relative concentrations between the

hydrofluoric acid etchant, HF, and the ammonium fluoride buffer, NH_4F. This work used an etchant with a 1:6 by volume ratio of HF (49% by mass) to NH_4F(40% by mass). The chemical reactions at work in the BOE process are the buffering reaction between HF and NH_4F that regulates the speed of the overall etch by controlling the amount of F^- ions in solution and the reaction between HF and SiO_2 that removes the oxide. Experience revealed that the BOE process removes SiO_2 at a prodigious rate (>10 nm/sec), so even the briefest of immersions is quite sufficient to remove any native oxide.

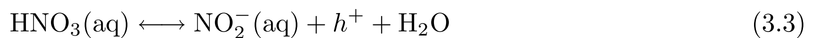


$$NH_4F(aq) \Longleftrightarrow NH_3(aq) + HF(aq) \tag{3.1}$$



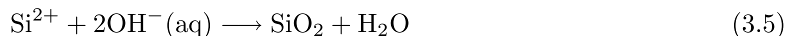
$$6HF(aq) + SiO_2 \longrightarrow H_2SiF_6(aq) + 2H_2O \tag{3.2}$$

Additionally, wet etches can be used to remove more than just surface oxides. Before the Rimberg lab had access to reactive ion etching (RIE), wet etch methods for removing SiGe were explored, drawing on prior experience with the success of wet etches for GaAs-based devices. [1, 12, 15] Ultimately, the anisotropy and slower speed of the RIE process allows for greater precision, but the wet etch is presented here for the sake of completeness, since the earliest generations of attempted devices used this technique. A variety of wet etches for removing Si exist, and several were tried during early investigations. The wet etch that proved most successful included nitric acid, HNO_3 as an oxidizing agent and hydrofluoric acid, HF to remove the oxidized Si. The presence of Ge and the strain induced in parts of the heterostructure lattice as a result accelerates the etch process, leading to higher selectivity for SiGe over Si, in about a 13:1 ratio. A simplified version of the chemical reactions governing this etch appear below, with Ge reactions excluded. [49–52]

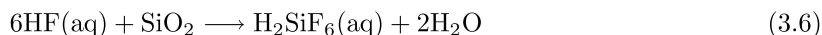


$$HNO_3(aq) \longleftrightarrow NO_2^-(aq) + h^+ + H_2O \tag{3.3}$$

$$Si + h^+ \longrightarrow Si^{2+} \tag{3.4}$$



$$Si^{2+} + 2OH^{-}(aq) \longrightarrow SiO_2 + H_2O \quad (3.5)$$



$$6HF(aq) + SiO_2 \longrightarrow H_2SiF_6(aq) + 2H_2O \quad (3.6)$$

Ignoring the presence of Ge still allows for a proper understanding of the etching process, given that Ge is minority component whose major effect is a source of defects that promote the reactions at work on the Si. In the first reaction, the holes (h^+) that form in the first step occur at a cathodic site on the Si surface before becoming part of the oxidation reaction of the Si occurring at a nearby anodic site in the second step. [49–52] As a final note regarding the viability of this etch, experience revealed that this chemistry, while compatible with photoresist, proved incompatible with the more delicate e-beam resist, even in the presence of standard adhesion promoters such as HMDS, hexamethyldisilazane, formula $(CH_3)_3$Si-NH-Si$(CH_3)_3$).

3.3.2 Reactive Ion Etching

Reactive ion etching (RIE) involves the use of gaseous species subjected to an electric field to form a plasma whose constituent ions are driven by microwave radiation to react with the material to be removed. Proper selection of gases and operating parameters serves a two-fold purpose: high chemical selectivity to etch one material preferentially and profile control in the etched region to achieve the desired aspect ratio. Given that high selectivity is also an advantage in a wet etch process, the latter reason constitutes the principle reason for implementing an RIE process, although chemical incompatibility between the wet etchant and the resist may also prompt the use of RIE. Standard operating parameters produce a highly anisotropic etch, with the borders of the etched region exhibiting nearly-vertical profiles, as this allows for finer resolution in the etched pattern. [53]

In terms of actual operation, the RIE process involves running the apparatus twice: once while empty to calibrate the system for the specific etch to be performed, and once again to etch the sample. Each RIE process involves five general steps: evacuate the chamber, turn on the gas flow,

wait for pressure to stabilize, expose the sample, and remove the sample to leave the instrument in standby mode. The specifics of this sequence appear in the paragraphs that follow. [53] For a complete picture, figure 3.8 depicts the RIE system schematically as well as a diagram of how the RIE process works on a sample already developed after a lithography exposure.

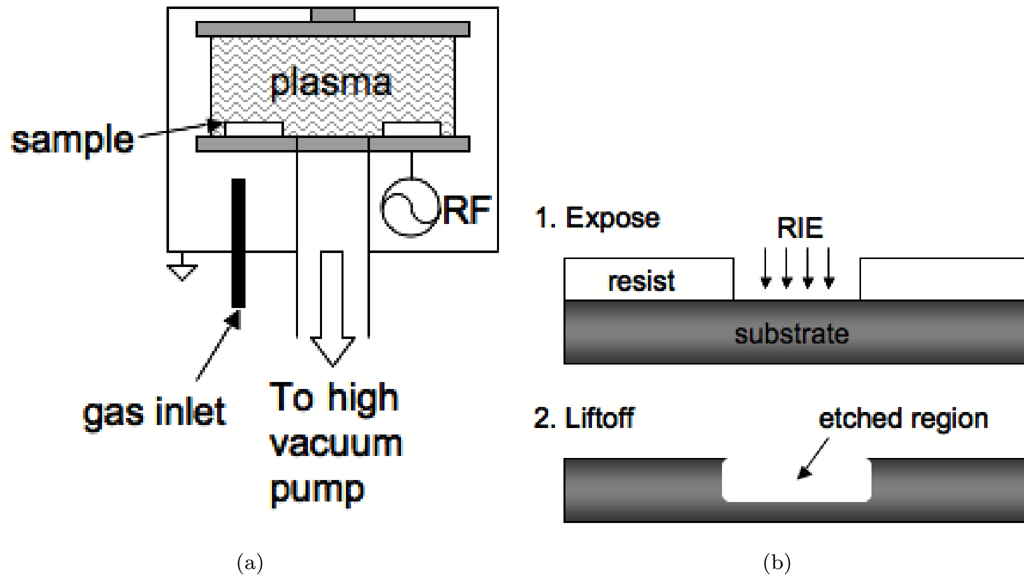
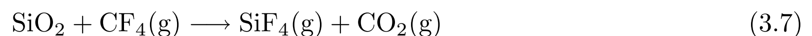


Figure 3.8 (a) Schematic of the RIE apparatus. (b) RIE process on a sample.

First, pump out the empty chamber by turning on the system, opening the main valve, and starting the pumpdown. The chamber pumps down first using a standard rotary vane mechanical pump until rough vacuum is achieved, at which point the turbomolecular pump takes over to achieve high vacuum. When the chamber pressure drops below $\sim 5 \times 10^{-5}$ Torr, turn on the flow meters and open the valves for the appropriate gas species. The turbopump will slow down its pumping speed to accommodate the gas flow. On this first empty run to tune the system, the pressure will likely be higher than intended, as the water vapor and other gases adsorbed to the chamber surfaces have not yet been removed. As a consequence, one should wait until the second run with the sample in place to make fine adjustments to the gas flow. [53]

After the pressure equalizes, usually around 10-20% higher than intended on this first run, set the exposure time to 3-5 minutes and activate the RF power. Adjust the forward power to the correct setting and tune the reflected power knob to minimize reflected power, preferably to 5 W or less. The reflected power knob actually tunes the frequency of the applied microwave radiation; at resonance with the plasma frequency, the reflected power is minimized. Achieving proper tuning is critical to a reliable etch process, as the plasma can oscillate chaotically when driven off-resonance, often resulting in a highly accelerated etch. Figure 3.9 illustrates the remarkable effect of an improperly tuned RIE process: the out-of-tune process etched a factor of 10 deeper than it should have for the recipe used. Experience reveals that the chamber tunes easily the first time when using only O_2, but processes requiring CF_4 work best with two tuning runs, with the chamber being pumped out again in between runs. After completing the tuning sequence, turn off the gas flows, vent the chamber, insert the sample, and pump down again. Proceed through the same sequence as above to perform the etch, taking the time to fine-tune the pressure after it equalizes with the gas flow on and resetting the time to the right value for the etch desired. The reflected power should remain minimized from the previous tuning exposure. [53]

The table below summarizes the operating parameters for each etch process and the etch rate, as confirmed by atomic force microscope measurements of the resulting etch depths. Further details about the SiO_2 etch appear in chapter 5, as this process became a necessary step in developing gates with reduced leakage currents. One can infer the chemistry of each RIE process from the information in this table: fluorine plays a crucial role in removing SiO_2, as in the case of the wet etch process previously discussed. The general reaction governing the breakdown of SiO_2 under exposure to a fluorocarbon plasma proceeds as follows:



$$SiO_2 + CF_4(g) \longrightarrow SiF_4(g) + CO_2(g) \quad (3.7)$$

Also, the oxygen ions readily react with whatever substance they bombard, oxidizing the exposed Si

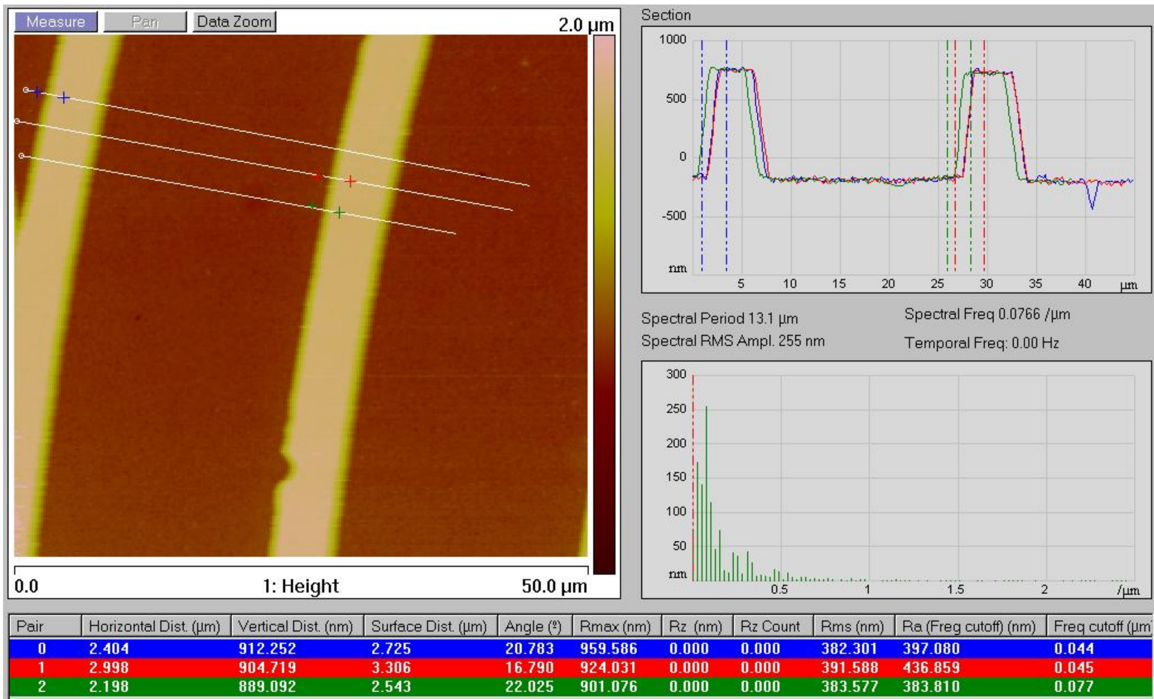


Figure 3.9 AFM image of results from an improperly tuned process. This etch recipe should have yielded an etch depth of 100±15 nm, yet it produced features an order of magnitude deeper.

Table 3.3 RIE Recipes

Process Name	Gas(es) Used	Flow Setting	Power (W)	Pressure (mTorr)	Time (s)	Rate (nm/s)
SiGe etch	CF_4 O_2	12.5 0.7	100	100	25	3.5-4.5
SiO_2 etch	CF_4	13.0	25	100	20	0.15-0.25
Resist De-scum	O_2	13.4	25	100	20	*

(or SiGe) surface, providing the SiO_2 for the above process to remove. Oxygen plasma also readily destroys organic compounds, such as the polymers in e-beam or photoresist. Using low power allows the oxygen plasma to "de-scum" the sample surface, breaking down any resist residue left after the development step in lithography, while leaving the unexposed resist mostly intact. [2, 54–56]

3.4 Cryogenics

One must employ various cryogenic techniques to freeze the free carriers out in a SiGe device so that the 2DEG behavior can be measured, to achieve superconductivity in Al/AlO$_x$ RF-SETs, or to observe Coulomb blockade in SiGe quantum dots. The following subsections detail three of these methods relevant to this work: liquid helium immersion, the dilution refrigerator, and the cryogen-free Heliox AC-V refrigerator.

3.4.1 Liquid Helium Immersion

Perhaps the most straightforward cryogenic technique is also the most intuitive: immersion in a bath of liquid cryogen, a process colloquially known as "dunking". A simple "dipstick"-style apparatus, also known as a "dunker", serves well for the purpose of establishing electrical connection from a sample immersed in cryogen to the room-temperature measurement electronics. As discussed previously, the excess free carriers in SiGe become energetically trapped at temperatures below ∼10 K, so dunking such devices in a bath of liquid He (T = 4.2 K) enables measurement of both ohmic contact performance and leakage current behavior. Dunking apparatus can range from the simple, such as a series of wires running down a pipe with coaxial connectors at room temperature and bare wires for pressed contacts to the sample at the bottom, to the complex, such as a dipstick combined with an evaporative cooling apparatus (known as a 1K pot when used in liquid He^4) allowing for temperatures colder than that of the cryogen bath and including coaxial cables for RF measurements. Figure 3.10 illustrates a basic dunker apparatus. For the sake of this work, the dunker used included DC wiring and, while equipped with a 1K pot, was only used while simply immersed in liquid He^4, achieving temperatures of just 4.2 K.

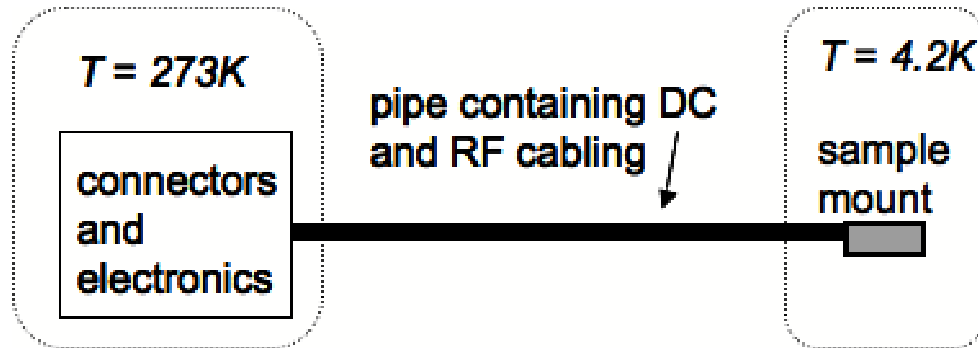


Figure 3.10 Schematic diagram of a basic dunker apparatus.

3.4.2 Dilution Refrigerator

After evaporative cooling a liquid cryogen, a process with a lower limit of about 250 mK, dilution refrigeration represents one of the most common ways of achieving very low temperatures. Dilution refrigeration exploits specific low temperature thermal properties of a mixture of ^{3}He/^{4}He, reaching temperatures of <10 mK. At very low temperatures, the properties of ^{3}He and ^{4}He are remarkably different. Liquid ^{4}He, a Bose fluid, experiences a superfluid transition below T = 2.18 K, becoming essentially its quantum mechanical ground state below 0.5 K. At the opposite end of the spectrum, liquid ^{3}He behaves as a Fermi liquid with high viscosity and a heat capacity that remains nearly linear with temperature. As a result, when a mixture of ^{3}He/^{4}He with more than 10% ^{3}He is cooled to less than 0.7 K, a spontaneous phase separation occurs, leading to the formation of a lighter ^{3}He rich phase and a heavier ^{4}He rich phase. This heavier phase bears the name "dilute phase", with the lighter phase referred to as the "rich phase", since the relative concentration of ^{3}He remains the important parameter. For ^{3}He concentrations near 10%, the phase separation occurs near T = 0.4 K, and the rich phase floats on top of the dilute phase without mixing, much like the case of oil floating on water. With decreasing temperature, the rich phase approaches 100% ^{3}He, while the dilute phase reaches a lower limit near 6.6% ^{3}He, resulting from the quantum mechanical behavior of these two very different liquids. The cooling process based on this phase separation is analogous to that of evaporative cooling, with the rich phase corresponding to the reservoir of liquid cryogen and the dilute phase being pumped on to achieve the cooling. Unlike traditional evaporative cooling, where the vapor pressure drops precipitously as $T \rightarrow 0$, ^{3}He migrates from the rich phase so that the dilute phase retains a concentration of 6.6% ^{3}He providing the vapor pressure for effective cooling even at temperatures of just a few mK. [1, 57–59]

The actual operation of a dilution fridge will now be discussed by referring to the schematic diagram of the apparatus illustrated in figure 3.11. By pumping on a small reservoir of liquid ^{4}He

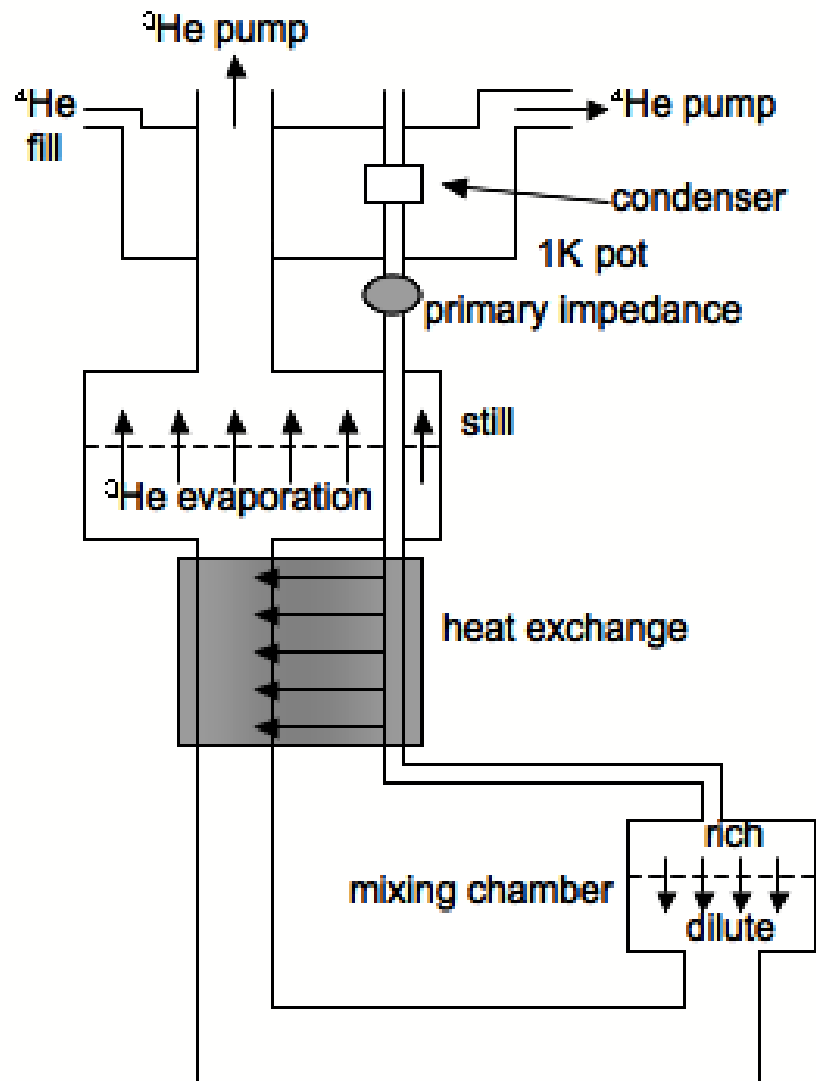


Figure 3.11 Schematic diagram of a dilution refrigerator.

connected to a large bath of liquid helium the 1K pot provides an evaporatively-cooled stage that achieves T $\approx$ 1.5 K, cold enough to liquefy the ^{3}He/^{4}He (15-20% ^{3}He concentration) gas mixture. An engineered impedance in the flow of mixture through the 1K pot guarantees condensation en route to the mixing chamber. High pressures maintained in heat exchangers and mixing lines maintain the condensed mixture in the liquid phase during this first stage of operation known as condensing. Once most of the available mixture condenses, circulation through the remainder of the system may begin. A room temperature closed-loop vacuum pumping system with cold traps controls the circulation flow while cleaning the mixture of impurities and preserving both the ^{3}He/^{4}He balance and the quantity of precious ^{3}He isotope. At the start of circulation the mixing chamber possesses a higher temperature than the still chamber, but this situation reverses after circulation progress and the mixture chamber starts to cool down. When the temperature of the mixing chamber drops below the critical point, phase separation occurs and the dilute phase extends all the way up into the still, enabling continuous cooling down to the base temperature of 5-10 mK by the process previously discussed. This work includes the use of the KelvinOx 400 dilution fridge available in the Rimberg lab, a high-access model with a cooling power of 350 μW and a base temperature of 7-8 mK. [1,15]

3.4.3 Heliox AC-V Refrigerator

The Heliox refrigeration system fulfills a niche between simple dunking experiments and the more complex dilution refrigerator by providing a cryogenic system with a base temperature of ~300 mK. This level of refrigeration results from a combination of pulse-tube cooler (PTC) and a standard ^{3}He refrigerator. Pulse-tube refrigeration, the details of which appear in the following paragraphs, draws upon an idea proposed by Gifford and Longsworth in 1966, although it only became technologically viable in recent decades. [60] The ^{3}He refrigeration works much the same as any evaporative cooler, with the exception that the precious ^{3}He isotope is retained in a closed-loop system, rather than

merely pumped away into the atmosphere. The Heliox system combines these two refrigeration processes in a clever way to achieve liquid cryogen-free refrigeration in a bench-top scale apparatus, making for a very economical choice. Given the relatively high base temperature and low cooling power when compared to a dilution fridge, as well as the lack of a superconducting magnet, the Heliox has some shortcomings. That being said, it serves well as a proving ground for prototyping new device designs and conducting certain measurements that do not require the lower temperatures, higher cooling power, or superconducting magnet available in a dilution fridge.

The PTC stages of the Heliox system provide the primary cooling power and are responsible for initially cooling the system down from room temperature to ∼2.5 K. The PTC refrigeration repeatedly cycles through adiabatic expansion of a compressed gas, lowering its temperature, followed by non-adiabatic compression through a regenerator to cool the system. A large porous mass with high specific heat serves as the regenerator, effectively dissipating most of the heat generated by the compression phase of the PTC cycle. The specific steps of the PTC cycle are as follows:

1. Helium gas is compressed in the pulse tube, raising its temperature.

2. The higher temperature gas is also at a higher pressure than gas in the reservoir end of the pulse tube, causing gas to flow into the reservoir, exchanging heat at the warm end of the pulse tube, dumping the heat into the surrounding environment.

3. The compressor system then adiabatically expands the gas in the pulse tube, lowering its temperature.

4. The cold, low pressure gas in the tube draws gas back out from the reservoir and heat is then exchanged at the cold end of the pulse tube, lowering the temperature of the cold stage in the Heliox fridge.

5. The cycle then repeats, starting with the gas being compressed in the pulse tube.

As depicted in figure 3.12 below, the Heliox system 2-stage PTC operates using a rotary valve that cycles repeatedly at a rate of about 80 times per minute, actuating both PTC's at once using a single compressor system. Working in series, the PTC's achieve a temperature of ∼2.5 K, cold enough to liquefy the charge of ^{3}He gas in the closed-loop evaporative cooler. Using a sorption pump, the liquid ^{3}He is slowly evaporated, cooling the final stage to ∼300 mK. Given that this closed-loop system has a fixed charge of ^{3}He gas to begin with, an upper limit on the operating time necessarily exist. Fortunately, in the case of this system, the hold time at base temperature exceeds two days (∼ 50 hours). Even better, although the system warms back up to a few K after the exhausting the liquid ^{3}He, recycling the charge occurs quickly, enabling continued operation at temperature after only 2-3 hours.

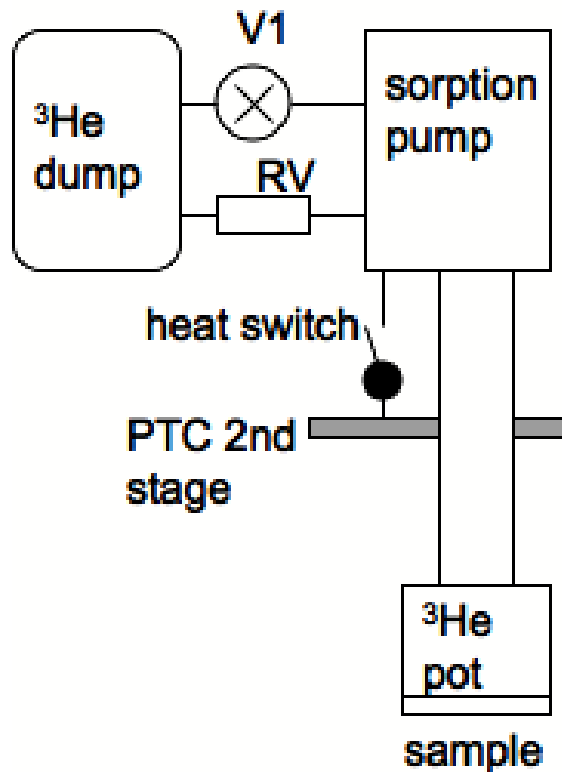


Figure 3.12 Schematic diagram of the Heliox AC-V refrigerator.

3.5 Measurements

After navigating all of the previously discussed methods in the correct order, the sample should be complete with a potentially working device and at the right temperature to perform the measurements of interest. The final section of this chapter presents the methods used to establish electrical connection to the sample and to perform both DC and RF measurements.

3.5.1 Static Protection and Wirebonding

Since mesoscopic devices such as quantum dots and especially RF-SETs exhibit high sensitivity to static discharge [1,12,15], one must take great care when connecting them to measurement apparatus. The use of instruments such as the wirebonder (a common tool in industry) to aid in connecting devices to the measurement apparatus can introduce additional layers of complexity that require further attention to the grounding situation. Reliable methods exist for protecting the sample during handling and wirebonding, several of which are listed below:

1. Always transport the sample inside a metallic box that functions as a Faraday cage, inside of which it remains effectively protected it from external static charges.

2. Use antistatic mats, gloves, tweezers, and grounding straps when handling and wiring the sample to significantly reduce the chance of accidental discharge.

3. Make use of lithographically-defined shorting leads between opposite ends of the device (later cut before taking measurements), make-before-break switches, and custom-designed plugs to short all connections to ground when wiring the sample to the apparatus.

4. Take care to insure that one's hands, tools, and the sample itself all remain at the same ground as the wirebonder.

Once properly grounded, the wirebonder proves itself an invaluable tool by improving bonding success over previous methods [1, 12, 15] and enabling smaller spacing between bonding pads, which allows for more devices per sample chip. The basic principles at work in the case of the wedge-bonder used in this work are quite straightforward. In preparing the bonder for use for, Al wire 25 μm in diameter and doped with $\sim$1% Si to provide the correct mechanical properties, must be properly threaded through a system of actuators and feed controls. Once in place at the end of a needle-like tool in mechanical contact with an ultrasonic transducer, one can use the manipulator arm of the wirebonder to bring the tool down to the sample surface, at which point the automatic functions of the semi-automatic bonding sequence take over to apply the correct amount of ultrasonic power and bonding force for the correct amount of time, as determined by user settings. If the bonding parameters are correct, the ultrasonic pulse melts small amounts of metal in the wire and the contact pad on the sample together, resulting in a strong electrical connection. After the first bond, the clamp controlling the wire feed opens and wire can be spooled out to traverse the distance to the second bond point, where the automatic sequence repeats and concludes the bond by breaking the wire afterwards and feeding a bit more wire through the clamps to position the new end under the tool. Thus, the bonder completes the cycle by readying itself to commence with a new connection. Bonding success depends on the cleanliness of the tool, the quality of the wire used, and the quality of the contact pad surface. Experience revealed that with the bonding force setting fixed, the bonds to Pd pads worked best with power settings of at least 450 and time settings of at least 75 ms, while the bonds to ohmic contacts and Al pads needed more ultrasonic energy delivered (power of 500 and 90 ms) and bonds to the thick gold contact pads on the measurement apparatus needed the least (power of 380 and 50 ms).

3.5.2 DC and Low Frequency Electronics

Direct measurement of the leakage current between the Schottky gates and the 2DEG constitutes the main DC technique performed in this work. The leakage current signal results from imperfect barriers forming between the Schottky gates, allowing potentials applied to those gates to cause current to flow to the 2DEG. The results of these measurements and the results of attempted solutions to the problem appear in chapter 5, along with a more thorough discussion of the phenomenon. The measurement of leakage current requires only a simple DC apparatus consisting of a custom designed voltage sweep box to ramp the potential on a Schottky gate, a custom designed current pre-amplifier to measure the leakage current amplitude, and a custom built voltage amplifier to serve as a buffer. As illustrated in figure 3.13, the current amplifier connects in series with the device, while the voltage amplifier is set to unity gain to serve as a buffer that helps solve a ground loop issue. Computer data acquisition using LabView software and DAC board hardware records the outputs of the outputs from the current amplifier and the voltage amplifier. Experience revealed that the computer and DAC board produced significant ground noise, so a custom built optoisolator circuit installed between the DAC and amplifier outputs proved successful at resolving this problem by separating the digital and analog grounds.

Four-probe lock-in techniques provide a convenient low-noise quasi-DC method of determining the conductance characteristics of a device. The apparatus illustrated in figure 3.14 was used to measure the performance of ohmic contacts as well as the conductance of QPC and quantum dot devices. A small amplitude ($\leq 100\mu$V) AC signal at relatively low frequency ($\sim$11 Hz) is applied to one of the ohmic contacts. A custom-designed voltage amplifier in differential mode is placed to measure the voltage drop across the device, dV, while the input to a custom designed current amplifier is placed in series with the device to measure the current though it, dI. Using standard four-probe techniques allows for the elimination of contact and cabling resistance from the measurements, while the lock-

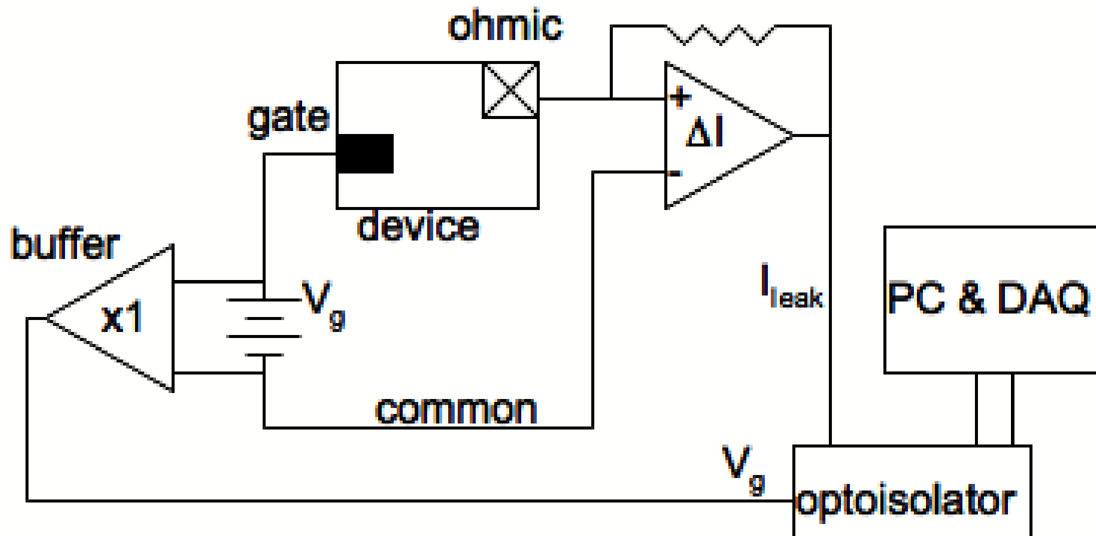


Figure 3.13 Schematic diagram of apparatus for measuring DC leakage currents.

in amplifiers measure the output of the current and voltage amps only at the signal frequency, reducing much of the noise. In the case of QPC conductance measurements, the potential on the Schottky gates is ramped using a custom voltage sweep box while the four-probe lock-in technique simultaneously measures the conductance through the QPC. For Coulomb blockade measurements of a quantum dot, the relevant QPCs are tuned near pinch-off and the potential of a plunger gate (an additional Schottky gate coupled to the dot) is ramped while the conductance through the dot is measured with the four-probe lock-in setup. Computer data acquisition using LabView software and DAC board hardware records the outputs of the lock-ins. Once again, a custom built optoisolator circuit installed between the DAC and amplifier outputs proved successful at reducing noise by separating the digital and analog grounds. [1]

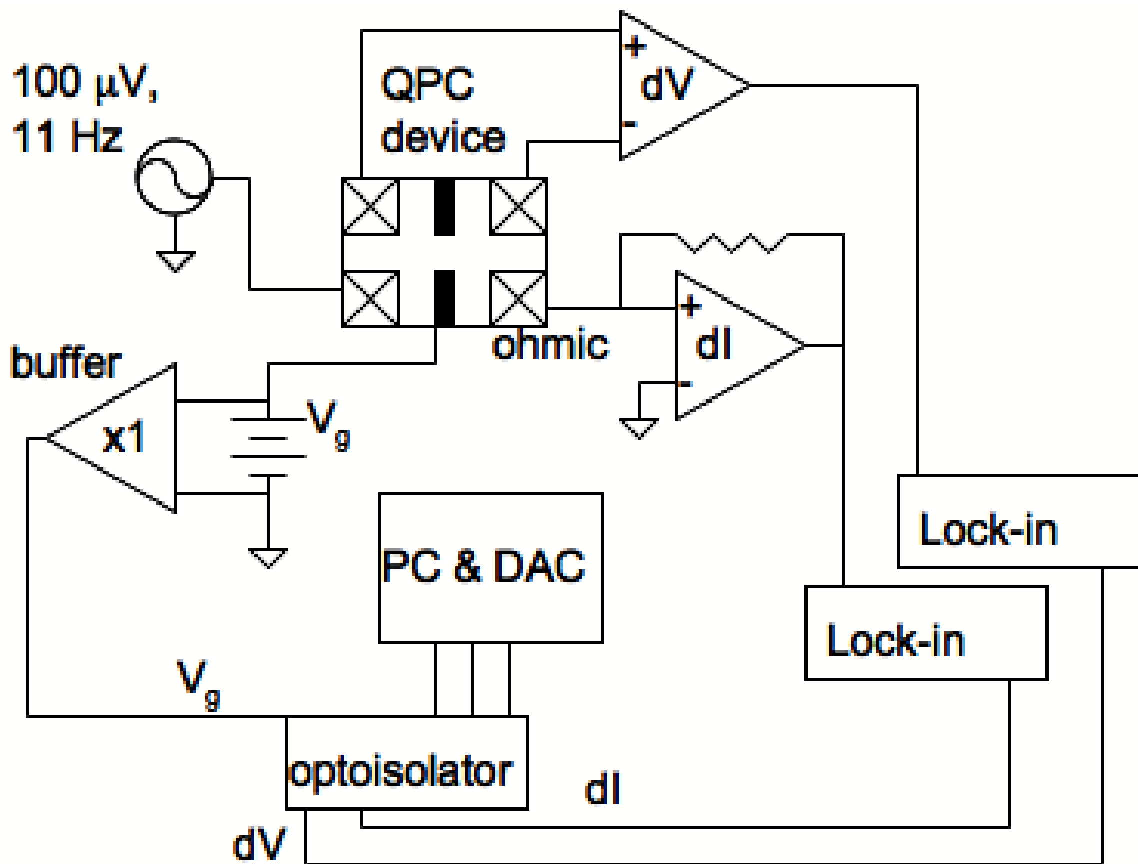


Figure 3.14 Schematic diagram of apparatus for 4-probe conductance measurements.

3.5.3 RF Electronics

Drawing on previous Rimberg group experience with RF measurements, reflectometry measurements characterized the high frequency performance of RF-SET devices fabricated on SiGe. To accomplish this, the device becomes part of a RLC tank circuit driven at or near resonance, as previously discussed in chapter 2. Figure 3.15 illustrates the RF setup as used in the dilution fridge where these measurements were performed. The first measurement performed determines the resonant frequency of the tank circuit and the change in reflectance as the device shifts into or out of Coulomb blockade. Using a network analyzer allows rapid sampling of the reflectance characteristics of the device over a broad frequency range, revealing both the resonant frequency and the amplitude modulation resulting from blockade. [1, 12, 15]

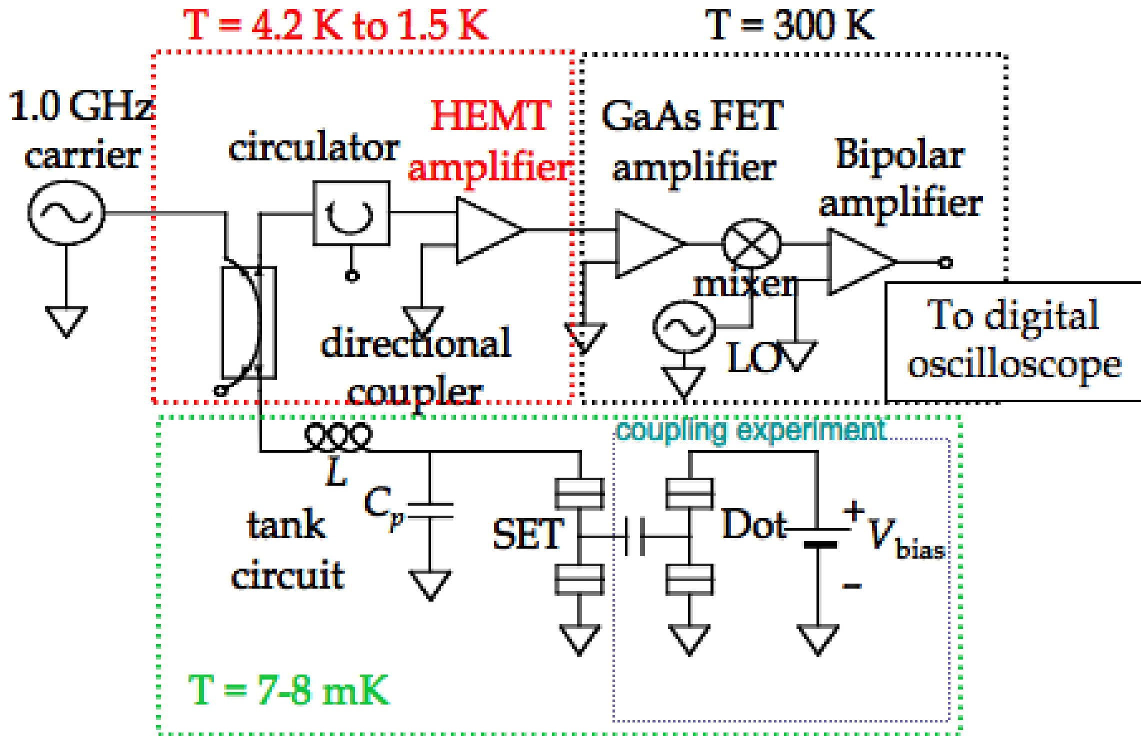
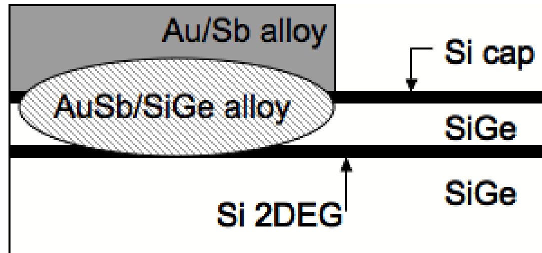


Figure 3.15 Schematic diagram of RF setup.

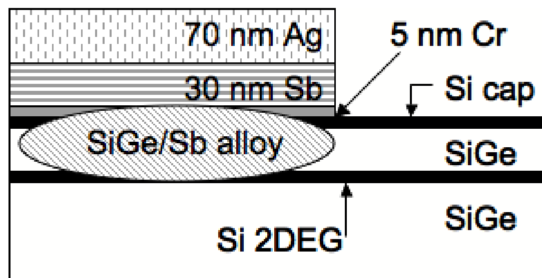
Chapter 4

Si/SiGe Materials Issues #1: Ohmic Contacts

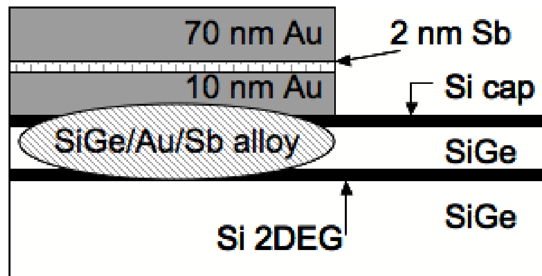
This chapter presents the investigation of several different approaches to forming ohmic contacts to the 2DEG in Si/SiGe devices, with the goal of developing a robust process with nearly 100% yield. The first section discusses the general model for diffusion in Si/SiGe as well as some of the key alloying processes at work in the ohmic contact recipes explored. The subsequent sections present the results of the different recipes investigated, including the specific steps in each procedure. Two competing materials combinations are routinely employed to make ohmic contact to Si/SiGe 2DEGs: Au/Sb and Ag/Ab. Figure 4.1 below illustrates the differences between three processes based on these two material systems explored in this work.



(a) Au/Sb alloy



(b) Layered Cr/Sb/Ag



(c) Layered Au/Sb/Au

Figure 4.1 Illustration of the three different ohmic contact metallization profiles.

4.1 Alloying and Diffusion in Si/SiGe

In general, the growth of ohmic contacts in a Si/SiGe heterostructure involves the deposition of various metals onto the bare Si surface of the cap layer (after removing the native SiO_2), followed by heating to a specific temperature for a specific amount of time. Two processes occur at the interface between metal and semiconductor during this anneal: alloying between metal and semiconductor and diffusion of metal donor atoms. Both of these processes result in increased conductivity by increasing the availability of charge carriers. This section discusses both of the relevant alloying and diffusion processes at work in the ohmic contact recipes explored later in the chapter.

Previous work on the fractional quantum Hall effect in Si/SiGe heterostructures provides some insight into the alloying processes at work in the growth of ohmic contacts in these materials. A eutectic alloy forms between Au and Si at 363°C and between Au and Ge at 356°C, and degradation of the low temperature performance of ohmic contacts formed from these alloys over time suggests that a Au-related defect mechanism could be at work. The fact that this degradation can occur at room temperature comes as no great surprise, given the relatively low eutectic temperatures. [26,61]

The other relevant alloying processes occur between Ag and Si and also between Ag and Ge, with eutectic temperatures of 845°C and 651°C, respectively. Given that it does not readily form a silicide, that it diffuses readily with both Si and Ge, that it accommodates large amounts of Sb as an intermetallic or interstitial without difficulty, and that it avoids spiking, a process where large grains of alloy penetrate deeply into the substrate, Ag proves itself a superb choice. Furthermore, the elevated eutectic temperatures suggest that any Ag-related defect mechanisms will be greatly suppressed at room temperature. [26]

In addition to alloying, the diffusion of the Sb dopant into the ohmic contact region plays a major role in the growth process. In diffusion, a random walk process, the distance a particle moves x scales linearly with the square root of time elapsed t and with the diffusion coefficient D,

a temperature-dependent quantity:

$$x = \sqrt{2Dt} \tag{4.1}$$

The diffusion constant itself generally depends exponentially on temperature T as follows,

$$D = D_0 \exp \frac{-E_A}{RT}, \tag{4.2}$$

where D_0 represents the maximum diffusion coefficient (at infinite T), E_A is an activation energy, and R is the universal gas constant. [62] A general model of dopant diffusion in Si provides additional details for the case of Sb in Si. In this numerical model, the diffusion coefficient has a more complicated dependence on both intrinsic and extrinsic parameters:

$$D_{Sb} = D_{Sb}^0 + D_{Sb}^- \left(\frac{n}{n_i}\right), \tag{4.3}$$

where $\left(\frac{n}{n_i}\right)$ represents a correction factor necessitated by the spatially varying Fermi level that depends on the relative concentration of ionized dopants and where

$$D_{Sb}^i = D_0 \exp \frac{-E_A^i}{RT} \tag{4.4}$$

for each $i = 0, -$. In the case of Sb diffusing in Si, this model provides for a correction factor to D ranging in magnitude from 1 to 2, depending upon concentration. [63]

Further enhancement to the diffusion of Sb occurs in the case of Si/SiGe heterostructures as a result of three effects tied to the fact that only vacancy point defects, and not interstitials, mediate the diffusion of Sb in Si and SiGe alloys where Si is the majority component. First, the presence of strain directly enhances diffusion by increasing vacancy point defect concentration. Second, the presence of Ge provides a "chemical effect" that also serves to increase vacancy defect concentration. Finally, both strain and the addition of Ge modify the band gap of the material in a way that can also enhance Sb diffusion. Large enhancements to the diffusion coefficient can result from this combination of factors: the ratio (with T fixed) D_{SiGe}/D_{Si} can exceed 200, resulting in enhancements to the distance

diffused great than a factor of 14. This unique combination of effects offsets the otherwise very slow diffusion of Sb as seen in pure unstrained Si. [64–70] Thus, through a combination of alloying and enhanced diffusion processes, annealed ohmic contacts can form conductive pathways through the Si/SiGe heterostructure to the buried 2DEG layer.

4.2 Approach #1: Au/Sb Alloy

Drawing on previous work by collaborators at the University of Wisconsin - Madison [22, 23], the first ohmic contact recipe tried involved the use of an alloy consisting of Au (99%) and Sb (1%). According to notes on the process received from collaborators, the basic steps involved were as follows:

1. Prepare the thermal evaporator by venting the chamber and loading the Cr and the Au/Sb alloy sources.
2. After developing the ohmic contact pattern laid down by photolithography, immerse the sample in BOE solution for 30 seconds to remove any native SiO_2 on the surface.
3. As quickly as possible to avoid oxide regrowth (< 90 seconds proves best), transfer the sample to the thermal evaporator and begin pumping down.
4. Evaporate 5 nm of Cr as an adhesion layer, followed by 80 nm of the Au/Sb alloy.
5. Liftoff in acetone to remove photoresist mask.
6. Anneal sample using a rapid thermal annealing (RTA) apparatus for 30 seconds at 100°C, followed by 30 seconds at 600°C.

Since RTA was not readily available in the Rimberg lab, the strip heater annealing method proven to work for ohmic contacts in GaAs [1, 12] became the obvious second choice. Several

attempts were made using the recipe detailed above, with the only difference being the annealing apparatus, but these met with no success. After some consideration regarding the differences in temperature measurement between the strip heater and the RTA, the possibility of a discrepancy became apparent. The strip heater uses a thermocouple spot-welded onto the resistive heater itself, providing a direct measurement of the temperature at the exact point of contact between sample and heater. In contrast, the RTA uses an optical thermal sensor that measures the average temperature of the whole wafer surface in the chamber; since the sample sits atop this other piece of wafer and represents such a small part of the area whose temperature is being measured, the device may well experience some deviation in temperature from what the RTA thermometer indicates.

Unable to quantify this variation easily, other annealing temperatures and times were systematically explored, ranging in time from 30 seconds to 5 minutes and in temperature from 380°C to 650°. In spite of a broad sampling of annealing parameters, none of the ohmic contacts grown using this approach yielded successful devices. Furthermore, since the Au/Sb evaporation source material is not a eutectic alloy, the coevaporation of these two metals may well produce a film vastly different in relative composition. [61] Given that Sb sublimates and that Au evaporates very controllably and reliably, this difference in composition seems likely and could well be contributing to the failure of this contact recipe. These disappointing results prompted further investigation into other recipes, the fruits of which appear in the following sections.

4.3 Approach #2: Layered Cr/Sb/Ag

The results of a literature search revealed that alternative ohmic contact recipes involving Sb and Ag (instead of Au) could also be successful and might have better overall yield at the outset as well as improved long-term reliability. [26,61] Also, after using another thermometer to confirm that the strip heater thermocouple was measuring the correct temperature, reliable reproduction of the

published annealing process could be achieved. Due to the different alloying temperatures of Si-Ag versus Si-Au, this new recipe required a higher temperature anneal. Additionally, since this recipe relies on the relatively slow diffusion of Sb through the Si/SiGe heterostructure, the anneal requires much longer times, as detailed in the procedure outlined below.

1. Prepare the thermal evaporator by venting the chamber and loading the Cr and the Au/Sb alloy sources.

2. After developing the ohmic contact pattern laid down by photolithography, immerse the sample in BOE solution for 15-30 seconds to remove any native SiO_2 on the surface.

3. As quickly as possible to avoid oxide regrowth (< 90 seconds proves best), transfer the sample to the thermal evaporator and begin pumping down.

4. Evaporate 3 nm of Cr as an adhesion layer, followed by 30 nm of Sb, and finish with at least 70 nm Ag.

5. Liftoff in acetone to remove photoresist mask.

6. Anneal sample using a resistive strip heater apparatus (with reducing gas flowing) for 1 minute at 110°C to remove any adsorbed water vapor, followed by 30 minutes at 600°C to form the ohmic contacts.

Providing sufficient time and temperature for the Sb to diffuse and thickening the Sb film to provide more material were the key changes from the process described in the literature. [61] Given that the 2DEG depth was more shallow in the devices described in the literature, such changes were necessitated. Initially, several different times and temperatures were explored, including some too short to yield ohmic contacts with acceptably low contact resistance. After some initial trial and error, this process eventually proved quite successful. The table below summarizes the results

Table 4.1 Ag/Sb Ohmic Contact Annealing

T (°C)	410	600	600	600	600	650
Time (min)	30	6	15	20	30	30
R (2-probe)	open	350-700kΩ	300-400kΩ	200-300kΩ	150-250kΩ	100-200kΩ

of these investigations, and also includes data from test anneals at 650°C. Although this higher temperature marginally improved the contact resistance, discussions with collaborators who grew the heterostructure revealed that the growth temperature of the material itself was close to the same temperature, so future ohmic contact growth was restricted to 600°C anneals to avoid damage to the 2DEG.

The four-probe resistance measurements of devices created with this recipe ranged around 1-5 kΩ, consistent with the mesa size of approximately 10 by 20 μn and 2DEG properties. Devices fabricated using this Ag/Sb ohmic recipe numbered into the dozens, and nearly all of the ohmic contacts (5 or 6 per device, depending on photolithography pattern) worked successfully. Experience revealed that a specific change of appearance in the metallization indicated successful ohmic contact growth. As depicted in the optical micrograph in figure 4.2 below, the mirrored finish of the topmost Ag film has changed to the ”melted” and perforated surface typical of a working contact.

Regarding the yield, routine failure modes explained those few instances of the odd device out: broken leads (due to bad photolithography) connecting the contact to the device mesa, broken wirebonds, and forgetting the essential BOE immersion step. Thus, the Ag/Sb ohmic contact growth process is inherently robust using thermally-evaporated metals. A slight variation on this recipe using the e-beam evaporator required the use of Ti instead of Cr for the adhesion layer, since Cr sublimates, but this altered approach met with failure. Further pursuit of e-beam evaporation for depositing the ohmic contact metals was subsequently abandoned, in light of the nearly 100%

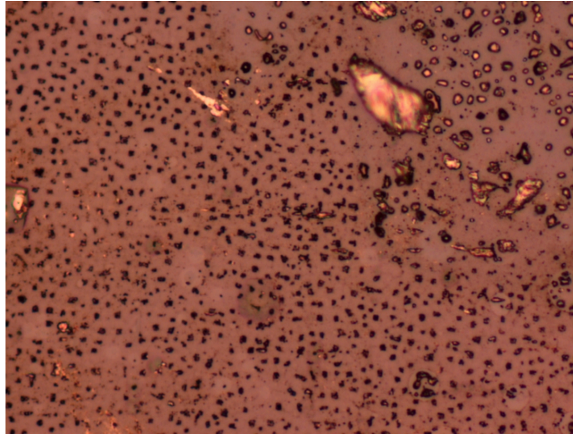


Figure 4.2 Optical micrograph of Ag/Sb ohmic contact surface, post-annealing. Samples annealed at 600°C for 30 minutes always exhibited this surface appearance when the ohmic contacts worked properly. The $\sim 5\mu$m square pit feature on the left side gives an idea as to the scale.

yield achieved using thermally-evaporated metallization.

In spite of this degree of success, however, continued concerns regarding the relatively long anneal at a rather high temperature (with respect to the growth temperature) prompted two more investigations: additional attempts with the Ag/Sb recipe, using the diffusive nature of the process to trade for a lower temperature by extending the anneal time, and a new variation on the Au/Sb approach based on the latest work by collaborators. The lower temperature trials with Ag/Sb became an undergraduate research project that has yet to offer up any results, although reasonable expectations based on the diffusion model discussed earlier suggest that temperatures as low as 500°C could yield successful ohmic contacts if given a sufficiently long anneal. The results of the revisited Au/Sb approach appears in the next section.

4.4 Approach #3: Layered Au/Sb/Au

The final method for growing ohmic contacts combined several desired properties in one successful process: nearly 100% yield, use of a strip heater instead of the RTA, and an annealing temperature well below the growth temperature of the material. Based on notes exchanged with collaborators, the following process was developed:

1. Prepare the thermal evaporator by venting the chamber and loading the three sources with Au, Sb, and Au.
2. After developing the ohmic contact pattern laid down by photolithography, immerse the sample in BOE solution for 15-30 seconds to remove any native SiO_2 on the surface.
3. As quickly as possible to avoid oxide regrowth (< 90 seconds proves best), transfer the sample to the thermal evaporator and begin pumping down.
4. Evaporate 10 nm of Au, followed by 1-2 nm of Sb, and finish with at least 70 nm of Au.
5. Liftoff in acetone to remove photoresist mask.
6. Anneal sample using resistive strip heater apparatus (with reducing gas flowing) for 1 minute at 110°C to remove any adsorbed water vapor, followed by 4 minutes at 400°C to form the ohmic contacts.

Over the course of dozens of devices spanning three different batches of material made using this ohmic recipe, essentially all of those processed correctly and devoid of any obvious flaws resulted in successful ohmic contacts. The two-probe resistances rangedfrom around 7 kΩ to almost 60 kΩ, and the four-probe resistances ranged from < 1 kΩ to about 10 kΩ. Not only are these values consistent with those expected for the given device mesa size and 2DEG properties, but they also indicate quite low contact resistances. Once again, experience revealed that successful ohmic contact growth

with this Au/Sb recipe resulted in the bright Au surface of the contacts transitioning to a perforated appearance similar to that seen in the case of Ag/Sb contacts. The optical micrograph in figure 4.3 illustrates this effect. Ultimately, the success of this lower temperature process and its ease of implementation with the strip heater led to its adoption as the primary method of ohmic contact growth for future devices.

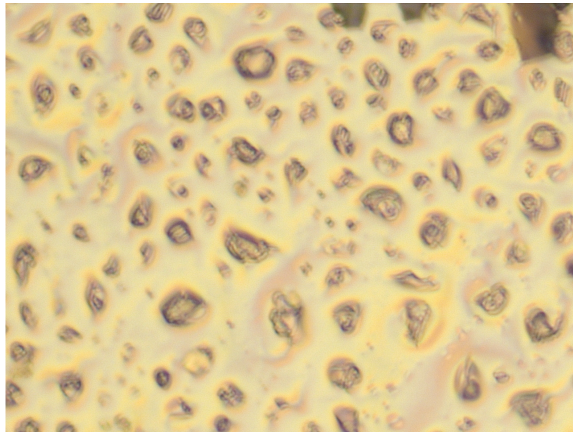


Figure 4.3 Optical micrograph of Au/Sb ohmic contact surface, post-annealing. Samples annealed at 400°C for 4 minutes routinely exhibited this surface appearance. The width of this field of view is approximately 90 μm.

4.5 Summary

Based on the models available for alloying and diffusion processes in Si and SiGe, the growth of successful ohmic contacts likely involves both effects. A phase transition from two separate species (metal and Si) in solid solution to a eutectic alloy formed of both occur, as does the diffusion of Sb, a n-type dopant in Si and SiGe, to produce an ohmic conductive pathway from the surface to the buried 2DEG. This work explored two robust ohmic contact growth recipes, one using layered Cr/Sb/Ag metallization annealed at higher temperatures (near the 2DEG growth temperature) for

longer times and another using layered Au/Sb/Au metallization annealed at lower temperatures for shorter times. Due to concerns about the elevated temperatures in the Ag/Sb process possibly degrading the 2DEG quality, the Au/Sb became the favored one for future devices.

Chapter 5

Si/SiGe Materials Issues #2: Leakage Current

This chapter presents the results of two approaches to solving the leakage current problem encountered when trying to form Schottky-gated devices in Si/SiGe 2DEG materials. Both of the approaches rely on the presence of a barrier oxide insulating layer; the differences lie with when that oxide is deposited in the fabrication sequence and the resulting changes to subsequent processing steps.

5.1 Problem Background

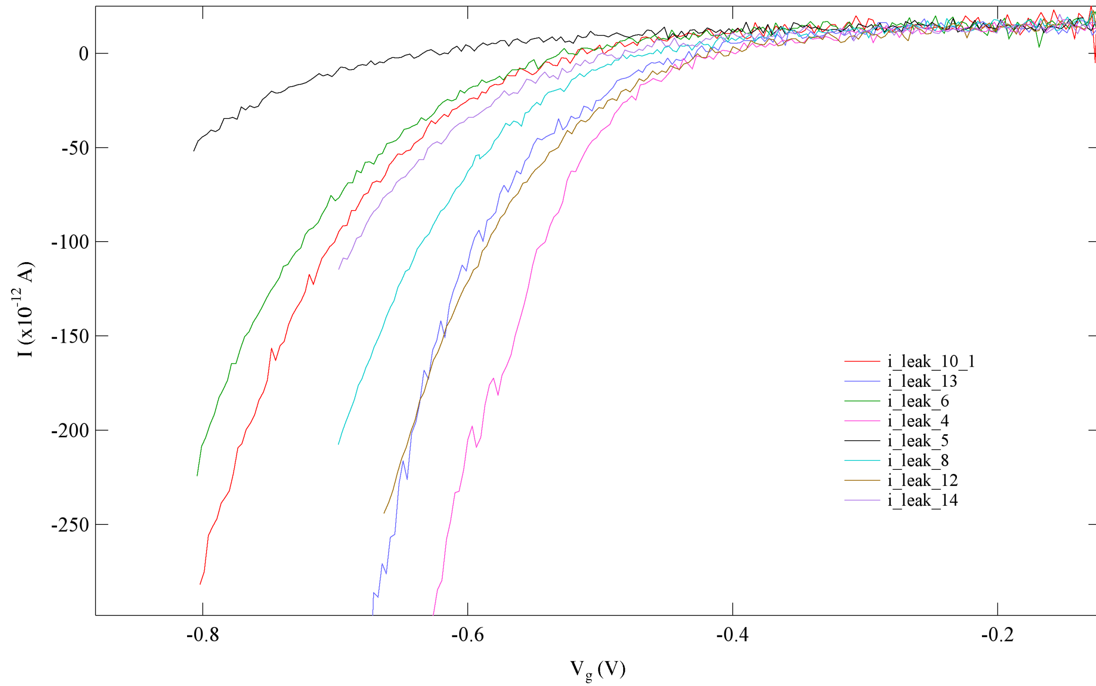
The presence of leakage currents, stray charge flow from the Schottky gates to the underlying 2DEG, remains an issue for many devices based on S/SiGe heterostructures. Several mechanisms present as likely contributors to the leakage current, including the pitting defects regular seen on the surface of the semiconductor including defects in the sidewall of the etched mesa that allow current to

traverse a region that should be depleted of charge carriers. Prior work with Si/SiGe devices using metallic Schottky gates favored two strategies for reducing leakage currents: minimizing gate area and etching away 2DEG under most of the gate metallization. [2, 19, 22, 23, 28]

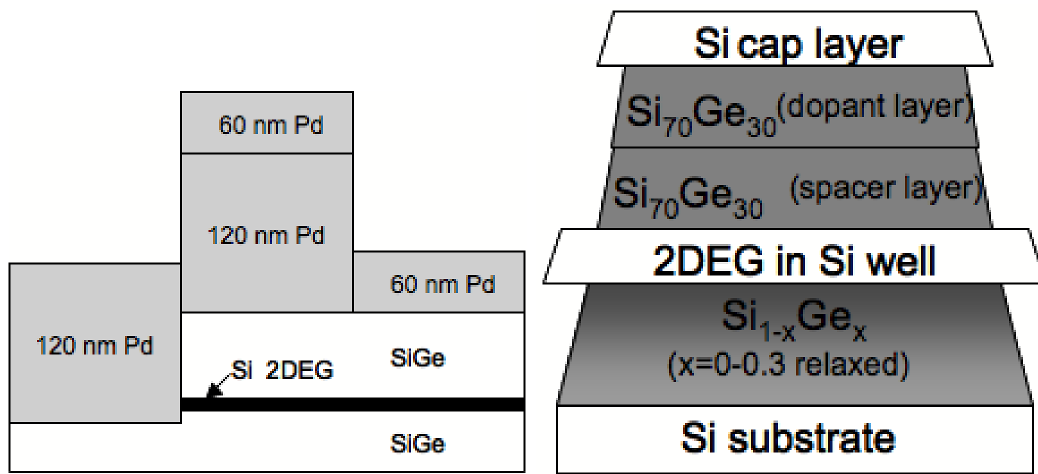
Measurements from devices fabricated at Dartmouth and employing just these two strategies for controlling current leakage routinely exhibited significant leakage behavior at relatively low gate voltages, often > -1 V_g. Additionally, most gates exhibited significant leakage current, while those few that did not leak appeared to be randomized in location around the mesa. Given that these early devices consisted of the entire quantum dot pattern, including both the large gate leads fabricated with photolithography and the small e-beam patterned device on top of the etched mesa, the exact cause of the current leakage phenomenon proved less obvious than initially anticipated. Considering this, a new batch of devices was measured both before and after the application of e-beam patterned Schottky gates on top of the mesa. These tests confirmed that the small area of these top gates did not contribute significantly to the overall current leakage behavior. Thus, the primary source of current leakage must come from the large photolithographically defined gates covering sidewall of the etched device mesa.

In addition to illustrating the device lithography in the vicinity of the mesa sidewall, figure 5.1 presents the leakage behavior of a typical device. Table 5.1 summarizes the results from multiple devices, with "Threshold Voltage" indicating the point at which the majority of gates began to exhibit leakage.

The results of these early tests made the case that the primary leakage current pathway occurred through the etch sidewall, prompting some reconsideration about the best approach to eliminating the problem. Since both prior strategies employed, etching away the 2DEG where possible and minimizing gate area on top of the 2DEG, address the problem of current leakage through pit defects, they necessarily become part of a successful strategy for controlling current leakage. They



(a)



(b) (c)

Figure 5.1 (a) Leakage current data from a typical device without barrier oxide. (b) Lithography profile for these early devices. (c) Etch profile from [2].

Table 5.1 Performance of Devices Without Barrier Oxide

Device	6/5	6/13	6/19	7/23	7/31	8/1	8/8	11/6
# Gates	5	8	10	10	9	10	10	9
Non-leaky	0	0	1	6	1	1	0	4
Leaky	5	8	9	4	8	9	10	5
V_{th}	-0.55	-0.5	-0.6	-0.3	-0.3	-0.3	-0.5	-1.5

are not sufficient on their own, however, since current leakage also occurs through the mesa sidewall, prompting the inclusion of additional fabrication steps that address this issue. Borrowing ideas and inspiration from the well-known industrial solution of employing a barrier region of insulator to stop current leakage, the following sections present the results of investigations into two variations on the theme of Schottky gates fabricated atop a barrier oxide. [19, 71]

5.2 Approach #1: Layered Schottky Gates

The simplest approach was tried first: depositing an insulating oxide layer as the first layer before depositing the metallization for the photolithographically defined large gate leads. For the sake of convenience, SiO_2 became the insulator of choice, as it was readily deposited using the e-beam evaporator. Other choices exist for the insulator and represent potentially fruitful directions for future projects that will appear in the final chapter. As can be seen in from the lithography profile diagram in figure 5.2, the presence of a thick oxide layer requires careful attention to detail to avoid breaks in the Pd metallization. Ultimately, this new process required three major modifications to pre-existing fabrication procedures: the addition of a thin Ti layer to allow the Pd to adhere to the SiO_2 underneath, the addition of an extra e-beam step to produce Pd ”patches” that insured the

continuity of the Pd film, and the implementation of a RIE process for native oxide removal, to be detailed in the subsection that follows.

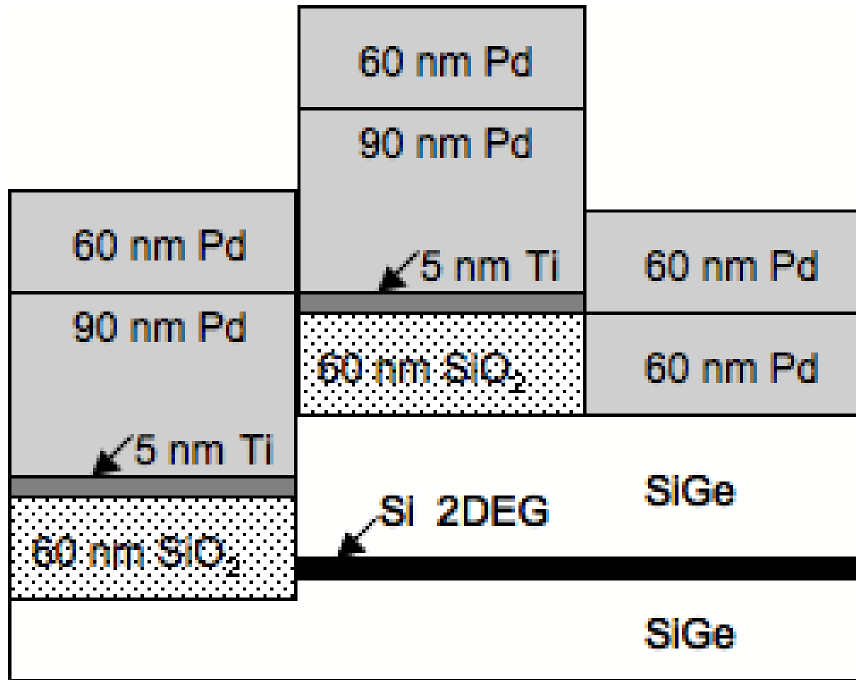


Figure 5.2 Diagram illustrating the lithography involved in creating Schottky gates with a layer of barrier oxide underneath. The SiO_2/Ti/Pd sandwich is fabricated using photolithography, and each successive layer of Pd represents an e-beam lithography step.

From figure 5.2, one can see that an oxide thickness of 60 nm and an etch depth of around 100 nm requires that the large gate pattern include >90 nm of Pd before the Pd layer even begins to approach continuity. As a consequence, two e-beam steps became necessary: the first one to deposit the Schottky gate pattern for the quantum dot on top of the mesa and including about 50 nm of Pd metallization and the second one to overlay large rectangular patches of Pd some 50-60 nm thick that spanned the overlap of photo and e-beam patterns. After the patching, a continuous layer of Pd became assured, especially since the oxidation of Pd between subsequent layers is almost

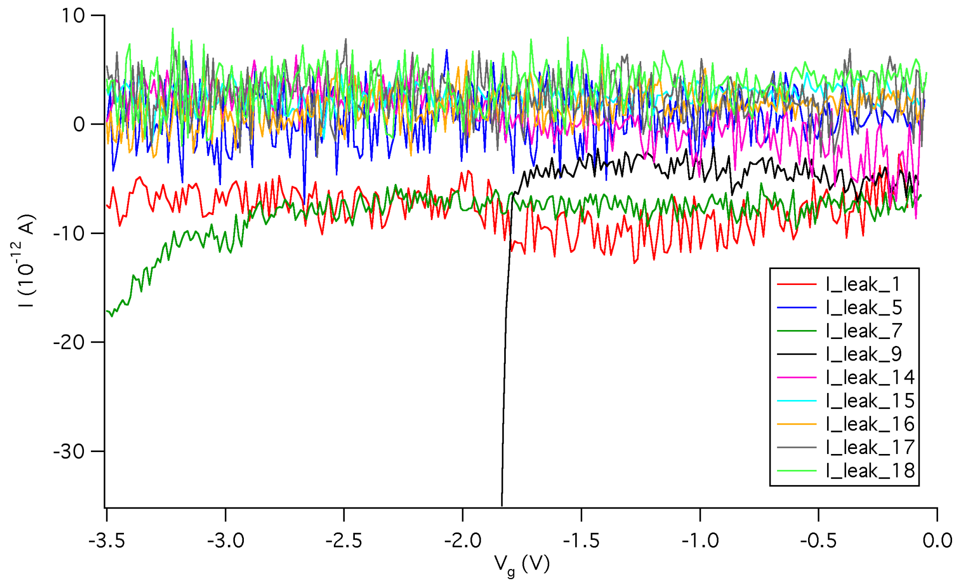
Table 5.2 Performance of Devices With Oxide Underneath Gates

Device	12/31	1/2	1/9	1/29	2/7	3/5
# Gates	12	12	3	12	8	8
Non-leaky	12	12	2	12	4	4
Leaky	0	0	1	0	4	4
V_{th}	$<$-3.5	$<$-3.5	-2.2	$<$-3.5	-2.5	-2.7

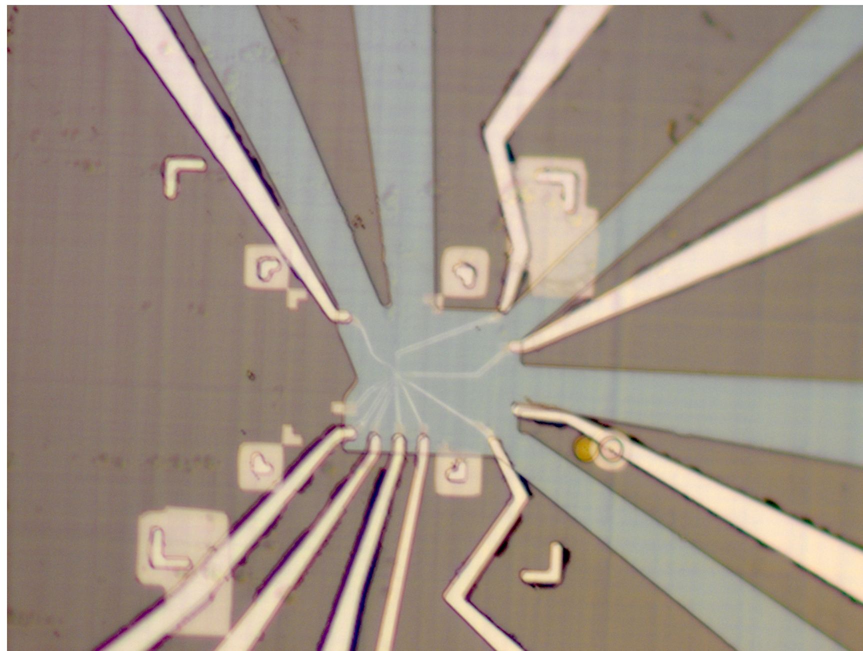
non-existant.

As for results, placing the barrier oxide under the gates in this fashion led to immediate improvements in the leakage behavior of these devices. Most all gates measured showed almost no detectable leakage current out to gate voltages of -3.5 volts, and a number of those were also measured at gate biases of -10 V with no detectable leakage current. Furthermore, the presence or absence of e-beam patterned gates had no obvious correlation to leakage current behavior. Those uncommon gates that did leak often did so at much larger gate voltages, with current leakage onset around -2.5 to -3 V, rather than -0.5 to -1 V. Those few gates with the worst leakage current characteristics (several hundred pA at gate voltages $>$ -1 V) were routinely found to be the result of lithographic error where scratched resist due to mishandling or the exposure of an alignment window resulted in a connection between the edge of the etched region and the gate metallization where one should not be. Figure 5.3 presents data from a typical device as well as an optical micrograph illustrating the sort lithographic error that led to leakage. Table 5.2 summarizes the data from a number of samples tested.

After a number of promising potential devices met with failure as a result of critical gates exhibiting the worst leakage current behavior due to lithographic errors, this method was abandoned in favor of backfilling the original photolithographically defined etch region with enough oxide thick-



(a)



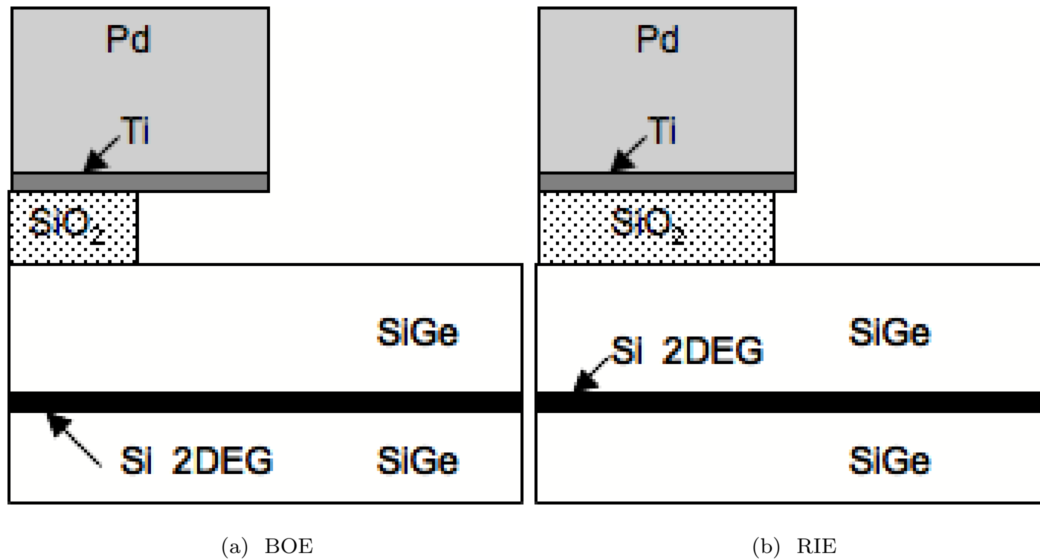
(b)

Figure 5.3 (a) Leakage current data from a typical device with barrier oxide deposited as part of large Schottky gate lead metallization. Each trace represents a different gate. These gates were not exposed to e-beam irradiation. (b) Optical micrograph of lithographic error on a different device, where the viewing window for the alignment marks overlapped the edge of the ohmic lead, resulting in leakage. The width of the device mesa is this figure is approximately 20 μm.

ness to block access to the edge of the 2DEG layer, where the leakage currents seem to originate. The results of this second approach appear in section 3.2 below.

5.2.1 RIE removal of SiO2

One key change from previous fabrication recipes came about as a consequence of depositing barrier oxides during the early photolithography steps: the use of BOE solution to remove native oxide before the deposition of the quantum dot Schottky gate pattern on top of the mesa had to be abandoned, as it would have also etched the barrier oxide. Figure 5.4 illustrates the contrast between BOE and RIE oxide removal processes on a system with oxide under the gates; the potential damage resulting from the isotropic BOE process is readily apparent, while the highly anisotropic nature of the RIE process should leave the barrier oxide largely intact.



(a) BOE (b) RIE

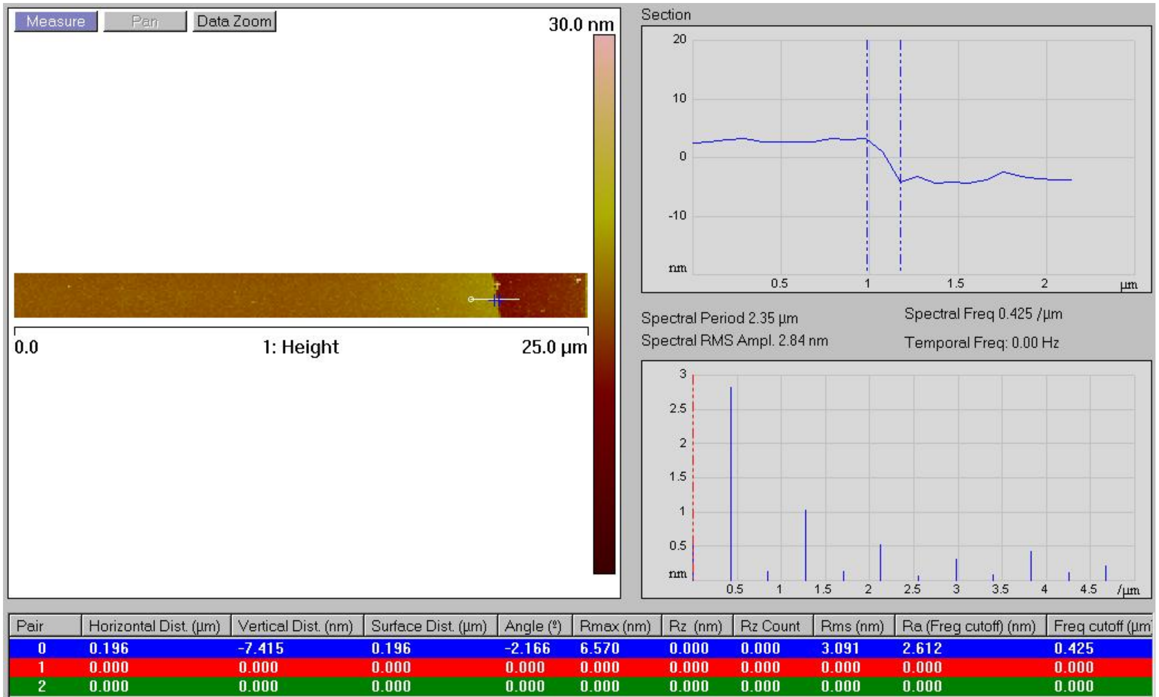
Figure 5.4 Important differences in oxide removal: (a) BOE removes SiO_2 isotropically, eating away the oxide under the gates, while (b) RIE is highly anisotropic, leaving the barrier oxide mostly intact while removing the native oxide.

As discussed previously in chapter 3, the removal of SiO_2 by a fluorocarbon plasma represents

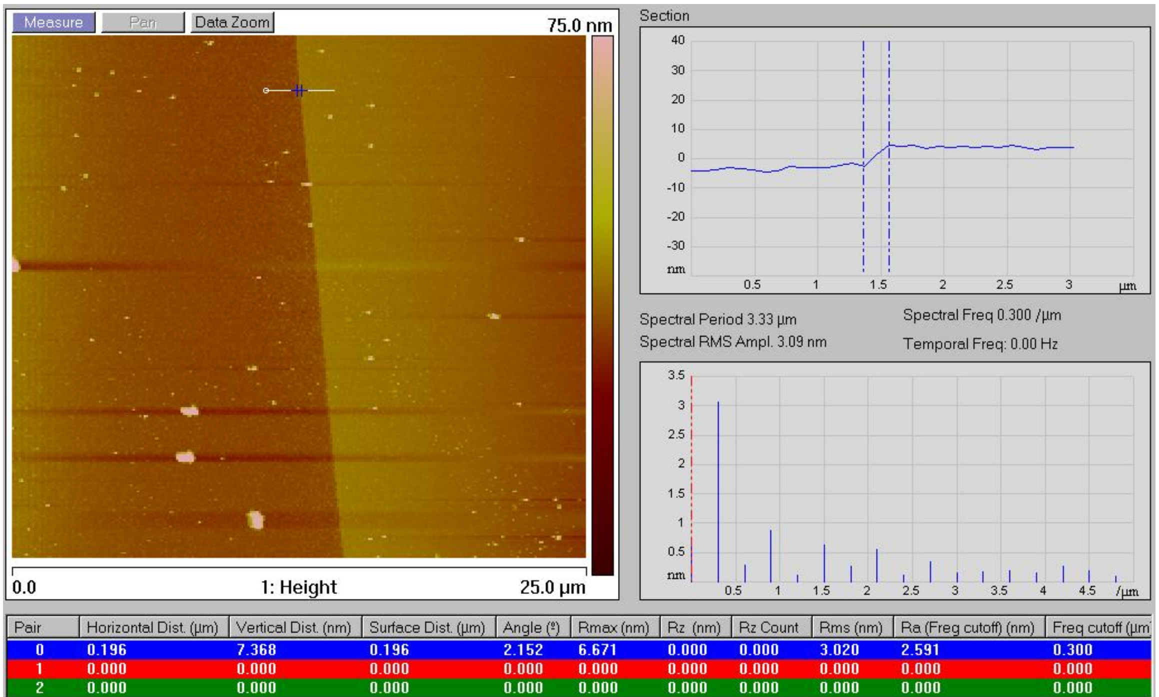
nothing new, but application of the process to the late stages of device fabrication was a new variation. Consequently, the etch process was explored in more detail with the intent of achieving a controllably slow etch for SiO_2 whose power low enough to leave intact both the underlying metallization and the e-beam resist mask. Prior experience with low power O_2 plasma cleaning revealed that a process occurring at 25 W resulted in only minimal (∼10%) widening of the pattern in the e-beam mask. Based on this, one could proceed with confidence that a 25 W exposure using CF_4 would produce no additional widening, as CF_4 should not react with e-beam resist at such a low power. [2, 54–56] Figure 5.5 below presents selected images and depth profiles from the AFM used to characterize this low power fluorocarbon etch of SiO_2 that became an essential part of device fabrication.

5.3 Approach #2: Backfilled Etch

With the general success of using a barrier oxide to reduce the leakage current problem, a slightly different tactic became necessary when lithographic errors were identified as a major cause of leakage in gates where the barrier oxide was present. Depositing an oxide to backfill the etched region stands as an alternative to the prior method of depositing oxide under the gates. Additionally, a properly deposited backfill places a barrier oxide around all parts of the etch sidewall, providing an additional layer of protection between the 2DEG and any future metallization steps, helping prevent leakage due to lithography errors. Given the need to use a Ti adhesion layer to allow the Pd to stick better to the underlying SiO_2, one must also deposit oxide during the Schottky gate leads photolithography process to insure that only Pd or insulator contacts the heterostructure surface, as Ti may not form a proper Schottky barrier with Si. A diagram illustrating the complete lithography profile appears in figure 5.6. As the figure indicates, the reduced thickness of oxide atop the mesa in the large photolithography gates allowed for the omission of the patching step seen in the previous approach.



(a) 30 seconds RIE



(b) 115 seconds RIE

Figure 5.5 AFM scans and profile sections illustrating the results of the RIE removal of SiO_2.

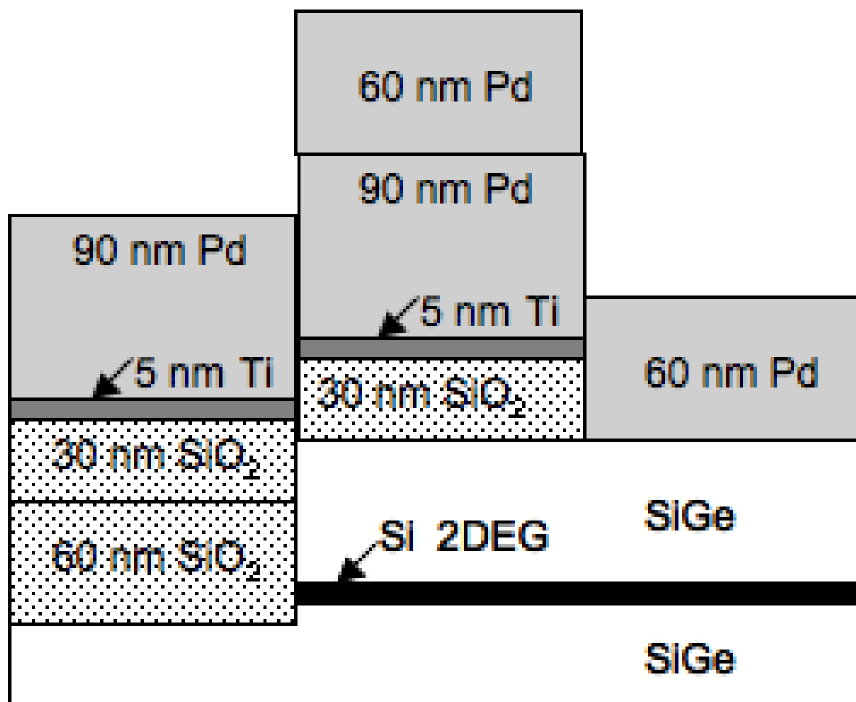


Figure 5.6 Diagram illustrating the lithography involved in creating Schottky gates atop a backfilled barrier oxide deposited immediately after the etch step. The SiO_2/Ti/Pd sandwich is fabricated using photolithography, and the subsequent layer of Pd represents an e-beam lithography step.

Figure 5.7 presents data from a typical device, and a summary of leakage current performance from multiple devices, all with backfill oxide thickness of 60 nm, appears in table 5.2. The table includes the number of gates measured per device, the number of those exhibiting current leakage, the number that did not leak, the average threshold voltage for the onset of current leakage, and the thickness of the oxide layer deposited directly under the large Schottky gate leads. Those with a (*) symbol next to the thickness indicates devices with e-beam patterned Schottky gates on top of the mesa; only these devices were exposed to e-beam irradiation before measurement.

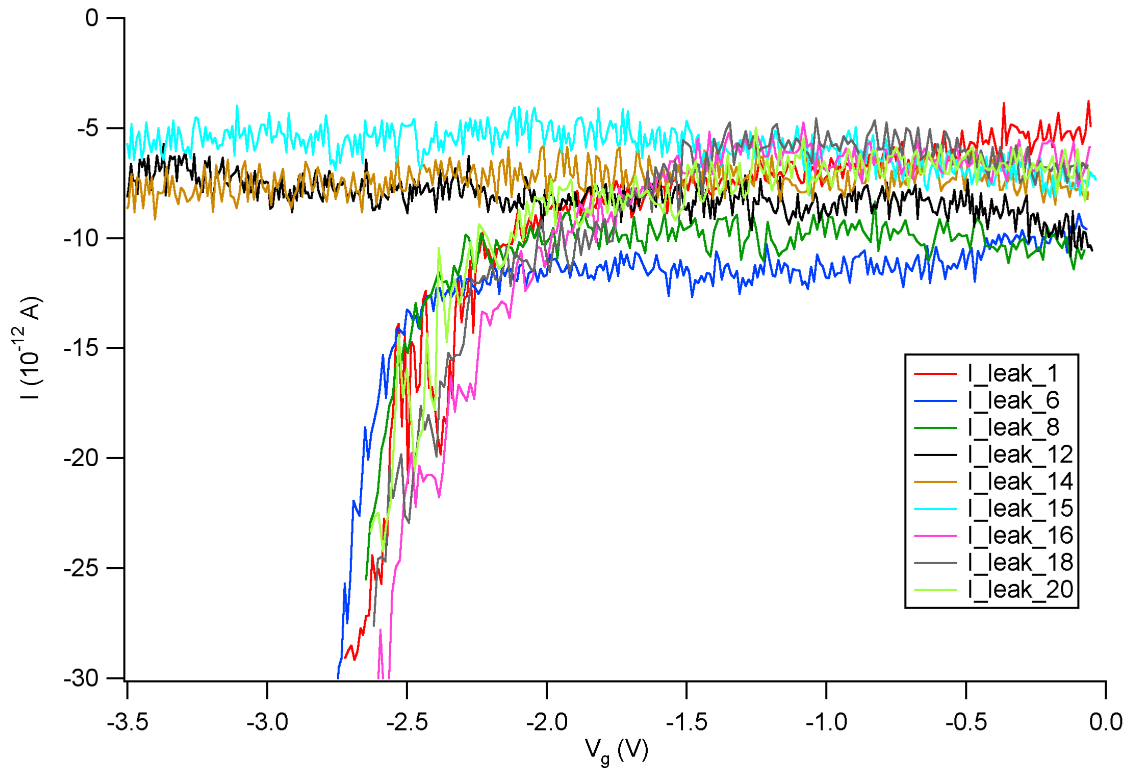


Figure 5.7 Leakage current data from a typical device with barrier oxide deposited immediately after the RIE step that defines the device mesa. Each trace represents a different gate, and those gates that leak were all subjected to e-beam irradiation in subsequent lithography steps.

As one can see from the data in the table, when the pattern was not exposed to e-beam lithog-

Table 5.3 Performance of Devices With Backfilled Etch

Device	3/20	3/21	3/30	4/2	4/5	4/16	4/18	4/25	4/27	4/28	5/7
# Gates	4	9	9	9	8	9	9	8	9	9	8
Non-leaky	4	9	8	4	2	3	4	4	4	5	3
Leaky	0	0	1	5	6	6	5	4	5	4	5
V_{th} (V)	$<$-3.5	$<$-3.5	-1.8	-2.5	-2.5	-2.5	-3.5	-2.7	-2.7	-2.7	-4.3
Oxide (nm)	5	5	5	5*	5*	5*	5*	5*	5*	5*	30*

raphy, this approach met with even better success than the earlier generation of devices where the oxide existed only under the gate metallization. Unfortunately, exposure to the e-beam during the addition of top gates causes some breakdown of the thin oxide on top of the mesa, leading to leakage currents occurring at smaller gate voltage values. Fortunately, the fabrication process permits use of a thicker oxide layer under the gates, and thicker barriers permit larger threshold voltages, pushing the onset of current leakage out beyond the point where pinch-off occurs in QPCs assembled from such gates. Additionally, changes in the photomask pattern and the subsequent alignment of the e-beam patterned gates to the mesa and large gate leads can prevent e-beam exposure of the edge of the mesa, potentially extending the threshold voltage even more. Furthermore, the oxide backfill can be increased to completely fill in the etched region, providing additional barrier oxide between the gate metallization and the mesa sidewall where the primary leakage current apparently originates.

5.4 Summary

The leakage current issue in Si/SiGe devices remains a problem that severely effects overall device yield at Dartmouth. Although etching away material to remove 2DEG where unnecessary and

minimizing the Schottky gate area on top of the device mesa reduces the effects of current leakage through pits and other surface defects, experiments suggest that the primary origin of the leakage current is through the sidewall of the etched mesa. Therefore, a strategy that employs a barrier oxide to block the leakage currents was implemented and proven to be successful. Two different approaches yielded encouraging results, and future generations of devices will likely find greatest success in a combined method: backfilling the entire etched region with oxide, depositing oxide under the large gate leads metallization, and taking additional steps during e-beam pattern alignment to avoid exposing the edge of the mesa.

Chapter 6

Devices in Si/SiGe

Once fabrication recipes for reliable ohmic contacts and Schottky gates with reduced leakage currents are in place, one can make steps towards integrating these changes with the pre-existing methods for realizing quantum dots (QDs) in Si/SiGe heterostructures. Also, with the goal of QDs incorporating integrated RF-SET charge sensors in mind, one must first complete proof-of-principle experiments showing that RF-SETs work as intended on Si/SiGe material. This chapter presents results from these experiments, starting with the RF-SET alone and then proceeding with QPC and QD experiments incorporating before discussing the progress made towards the integration of the RF-SET with a quantum dot.

6.1 RF-SET on Si/SiGe

Using the e-beam lithography and shadow evaporation methods detailed in chapter 3, one can fabricate SET devices consisting of Al/AlO_x tunnel junctions on a Si/SiGe substrate containing at 2DEG. As a proof-of-principle test, the SET devices were created on a bare Si/SiGe sample, without any additional processing steps beyond simple cleaning. Completing this sort of baseline

testing serves as a critical step along the way to future progress: if the RF-SET fails to work on Si/SiGe for some unforeseen reason, that would severely hamper the development of an integrated QD/RF-SET device.

The SEM micrograph in figure 6.1 depicts the actual device measured. Fabricated by shadow evaporating Al, using ∼16 nm for the first layer and ∼26 nm for the second layer, with a ∼3 minute oxidation exposure in between, this device exhibited a resistance $R_N \approx 215k\Omega$ at the ∼7 mK base temperature of the KelvinOx 400 dilution fridge.

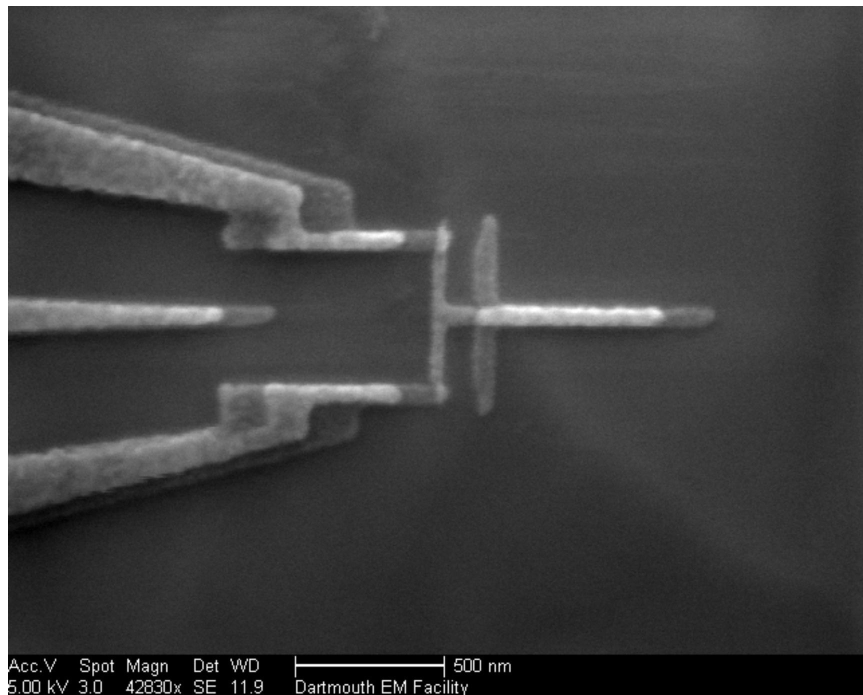


Figure 6.1 SEM micrograph of RF-SET fabricated on SiGe. This is a picture of the actual device measured.

Further characterization of this device using the sort of DC measurements described in chapter 3 produced the data appearing in figure 6.2. As the $I-V$ curve demonstrates, the zero-current region spans from approximately -0.75 to +0.75 mV, indicating a superconducting gap $\Delta \approx 187$ μV,

a value consistent with prior devices on GaAs heterostructures. [1,12,15] The Coulomb blockade oscillations exhibit a periodicity of ∼0.18 V. From these measurements, one can deduce that that both tunnel junctions of the device are intact and that the S-SET operates as expected, prompting the RF measurements to follow.

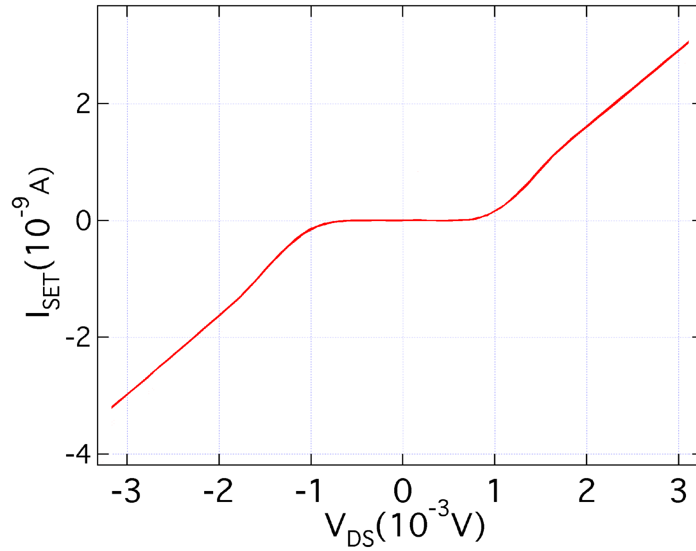
Applying the RF reflectometry measurements from chapter 3 to this device resulted in the data appearing in figure 6.3. The reflected power data, measured using a network analyzer, shows the modulation in reflected voltage at the tank circuit resonance frequency for the device both in and out of Coulomb blockade. The tank circuit parameters included an inductor $L \approx 70$ nH and a parallel capacitance $C_p \approx 0.35$ pF. The other measurement, performed using a spectrum analyzer, presents the modulation response of the RF-SET to the application of a $0.3e$ amplitude 100 kHz signal. The device response exhibits sidebands exactly 100 kHz on either side of the carrier wave at the resonance frequency of 1.02 GHz.

Based on these measurements, the RF-SET works as designed on Si/SiGe heterostructure material. Therefore, further progress towards an integrated QD/RF-SET system will be possible. The remainder of this chapter discusses those results obtained along the way to that goal.

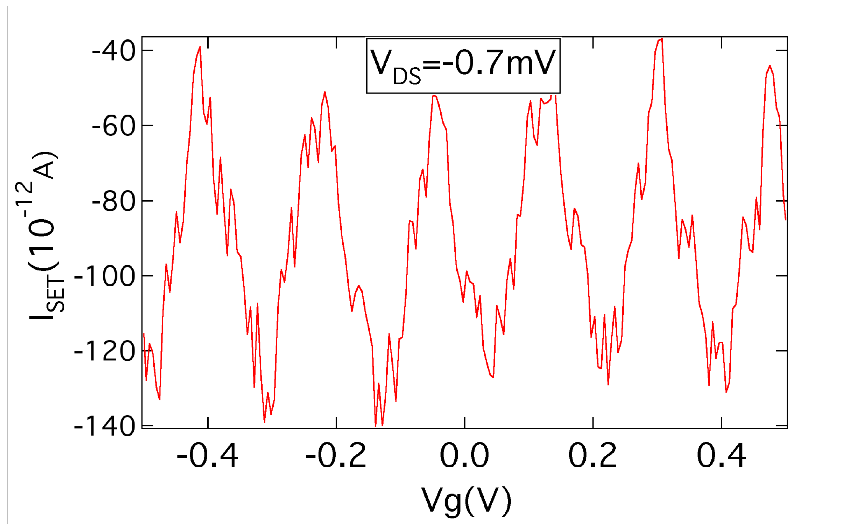
6.2 QPCs in Si/SiGe

The demonstration of successful QPC formation has been achieved by collaborators in relation to their successful demonstration of QD formation and valley-splitting characterization in Si/SiGe devices. [20,22,23,28] This work produced similar results in systems both with and without barrier oxides in place, demonstrating both reproducibility and the ability to achieve pinch-off in devices with barrier oxides. A sampling of these results appear in this section.

The behavior of QPCs formed from gates without barrier oxides in place routinely exhibited pinch-off after the onset of leakage current in these devices, resulting in residual currents after

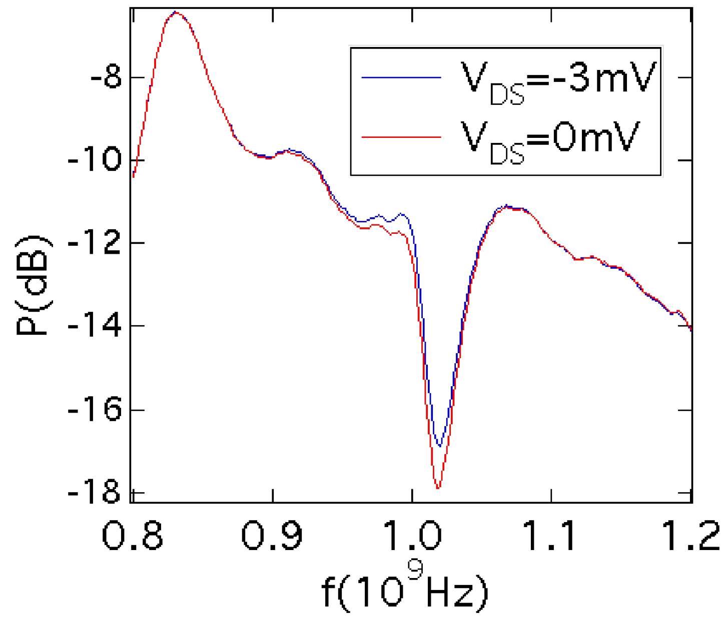


(a) $I - V$ curve

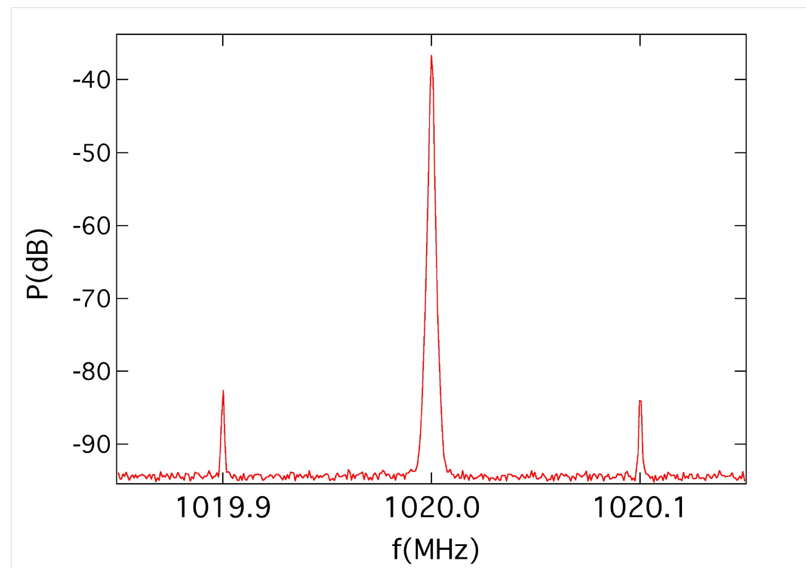


(b) Coulomb blockade

Figure 6.2 DC performance of the SET with R_N = 215 kΩ showing the superconducting I-V curve and Coulomb blockade oscillations.



(a) Reflected power



(b) Modulation

Figure 6.3 RF performance of the SET showing (a) reflected power in (red) and out (blue) of Coulomb blockade as well as (b) the modulation of the 1.02 GHz carrier wave with a 100 kHz 0.3e signal applied to the capacitively coupled gate.

"pinch-off" due to the open leakage channel. This residual leakage current signal was typically quite noisy. The data appearing in figure 6.4 represents a typical device, including the leakage current and QPC conductance measurements. Pinch-off for this device occurs around −2 V, and pinch-off in similar devices ranged from around −1 V to larger than −3 V, depending on the batch of material used and the presence or absence of nearby defects.

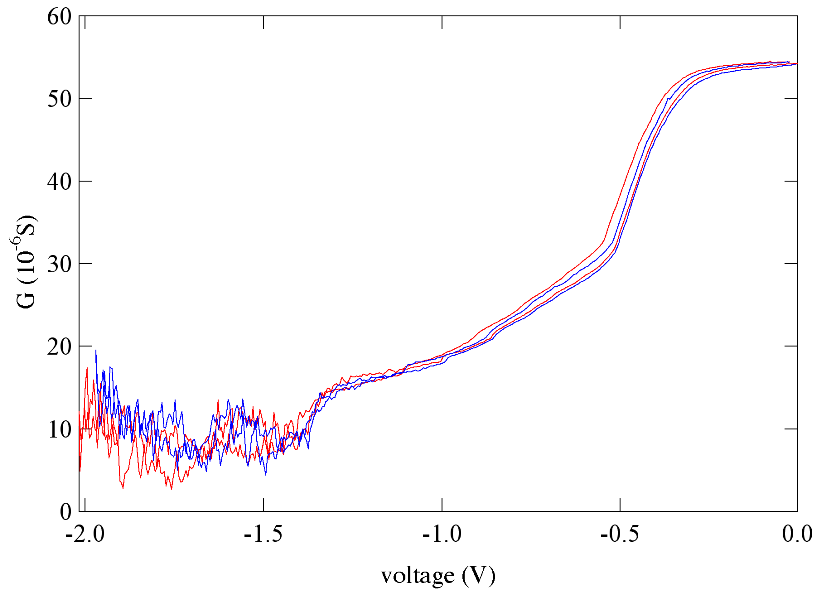


Figure 6.4 Plot of the conductance vs. gate voltage behavior of a typical QPC device without barrier oxides under the gates. Red and blue traces represent two different QPCs on the same device with a common gate between them. Leakage current noise overwhelms the pinch-off behavior below $V_g \approx -1.4V$.

More promising results came from the measurements of QPCs formed from gates with barrier oxides in place underneath. Leakage current in many of these devices began only after the QPC achieved pinch-off. The leakage current and pinch-off behavior of a typical device appears in figure 6.5.

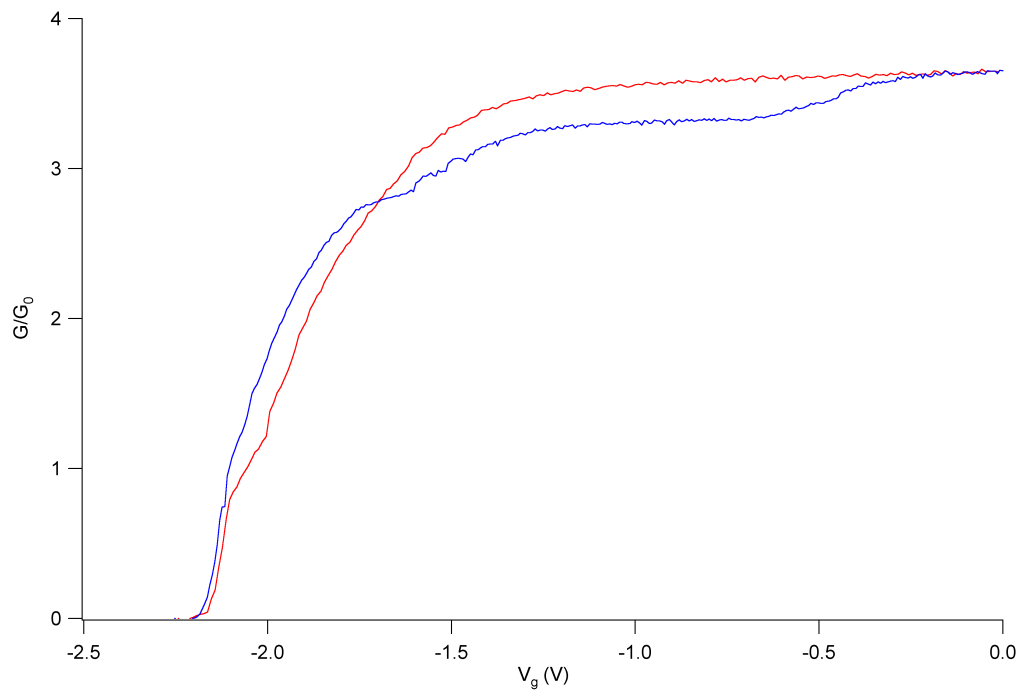


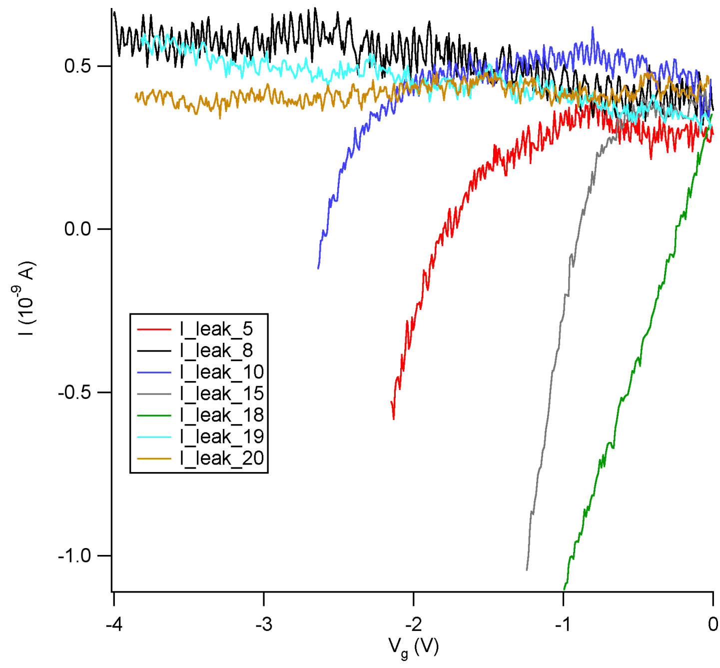
Figure 6.5 Plot of the conductance vs. gate voltage behavior of a typical QPC device with barrier oxides under the gates. Red and blue traces represent two different QPCs on the same device with a common gate between them. This device exhibited leakage current behavior in the dot-forming gates for $V_g < -2.75$, due to the e-beam exposure of the thin (5 nm) barrier oxide at the mesa edge.

6.3 QDs in Si/SiGe

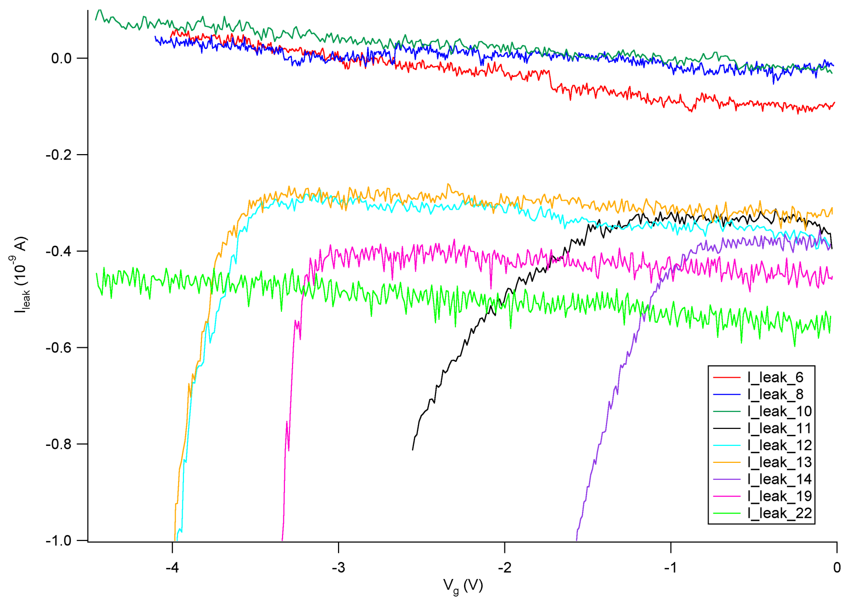
While QDs have been successfully achieved Si/SiGe before, including few- and single-electron dots by collaborators [22, 23, 28], this work presents the results from efforts to achieve a QD in a device with barrier oxides in place to reduce the effects of leakage currents. Both devices 5/4 and 5/11 exhibit leakage currents in several of the gates used to form the dots, as can be seen in figure 6.6.

In the case of device 5/4, with only 5 nm of SiO_2 between the large gate lead metallization and the edge of the mesa, the leakage from some of the gates forming the dot (5, 10, 18, 19, 20) is likely due to the degradation of the thin barrier oxide by e-beam exposure, consistent with the results presented in chapter 5 for other devices from the same sample chip. For device 5/11, the leakage current onset for those gates forming the dot (6, 12, 13, 14, 19) mostly occurs at larger gate voltages, consistent with the thicker 30 nm oxide layer under the large gate leads that go over the edge of the mesa. Device 5/11 also exhibited misalignment in the photo pattern that resulted in a gap in the barrier oxide and e-beam exposure at the mesa edge, both likely contributors to the excessive leakage on certain gates. Future generations of devices will include extra steps to compensate for this photolithography offset, leading to fewer leakage current issues. In spite of these leaky gates, conductance measurements were conducted on the available QPCs, with those from device 5/4 exhibiting pinch-off and those from device 5/11 failing to pinch-off, instead displaying strong noise in the current through the QPCs after the onset of current leakage. The results of these conductance measurements are presented in figure 6.7.

Finally, in the case of device 5/4, the QPC behavior appeared encouraging enough to attempt formation of a quantum dot. The Coulomb blockade data from this device appears in figure 6.8. The periodicity is $\approx$0.25 V, and the repeatability is high, after compensating for a small offset in $V_g$between the measurements.

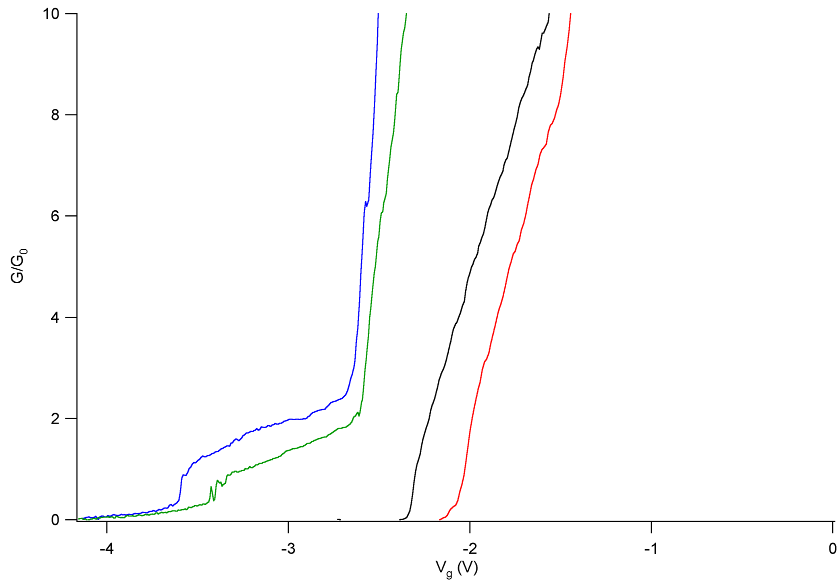


(a) Device 5/4

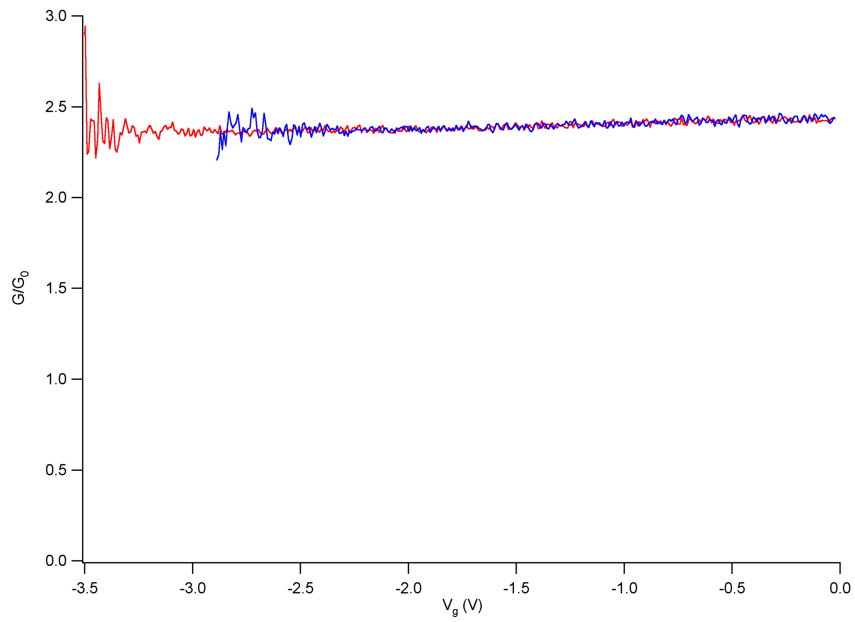


(b) Device 5/11

Figure 6.6 Leakage current performance; a small offset in the current amplifier is responsible for the non-zero baseline seen in (a) and the shifting baseline seen in (b).

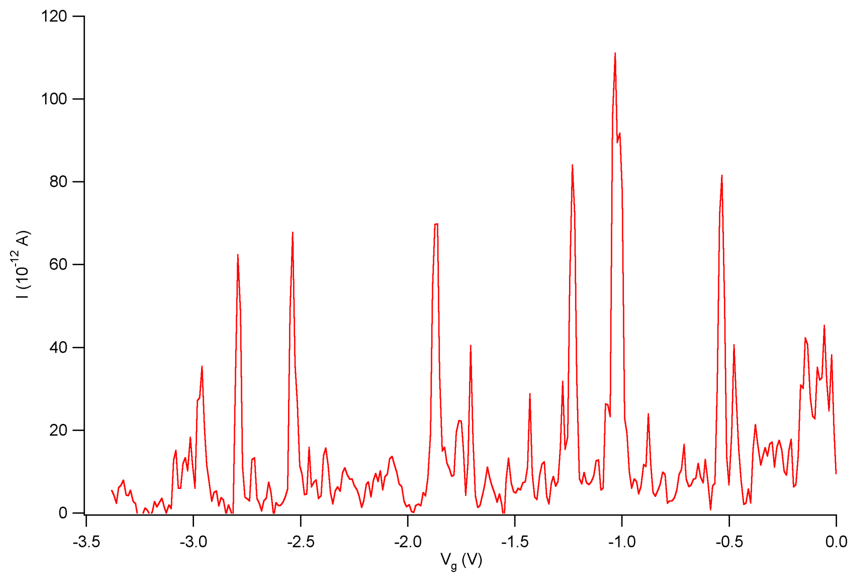


(a) Device 5/4

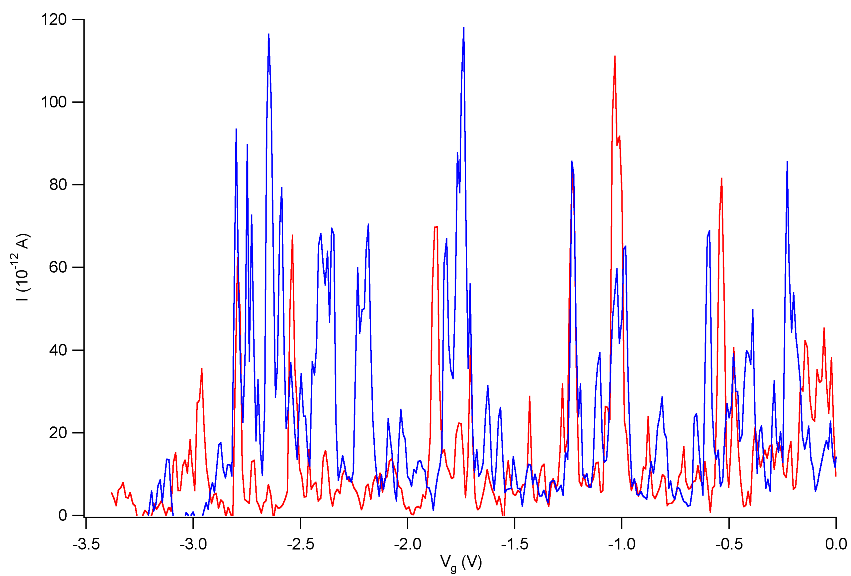


(b) Device 5/11

Figure 6.7 QPC performance. Device 5/11 failed to show pinch-off due to leakage currents caused by lithographic errors. Device 5/4 shows pinch-off in spite of the large leakage current on gate 18



(a) Coulomb blockade oscillations (CBO)



(b) CBO Repeatability

Figure 6.8 (a)CBO in a Si/SiGe quantum dot formed by Schottky gates with barrier oxides underneath. (b)Repeatability in successive measurements (blue) was strong, apart from a small offset in gate voltage (≈ 0.185 V, already corrected in the plot).

6.4 Integrated QD/SET and Double QD systems in Si/SiGe

As discussed in chapter 1, future qubit experiments in Si/SiGe require devices that incorporate charge sensors as readout devices on devices containing double quantum dots. This work included efforts in those directions, with lithography patterns developed for double QD devices with integrated charge readout through both QPC and RF-SET charge sensors. As can be seen in figure 6.9, the QD devices discussed in the previous section both included an integrated RF-SET charge sensor, but neither of these RF-SETs were intact by the time they were measured at the base temperature of the Heliox AC-V fridge.

Figure 6.9 SEM micrograph of a combined SET/QD device on Si/SiGe. This is a picture of the actual device that exhibited Coulomb blockade oscillations in the dot. In spite of appearing intact, the SET measured as an open-circuit.

Given that the RF-SET fabrication recipe developed for these final experiments produced dummy

devices with R_n ranging from about 35 to 60 kΩ with a yield in excess of 80%, statistics favors success in future generations of devices. Furthermore, those future devices incorporating the double QD pattern seen in figure 3.10 will also include an integrated QPC charge sensor, adding to the amount of information that can be gleaned from a device or providing redundancy should one of the two readout devices fail.

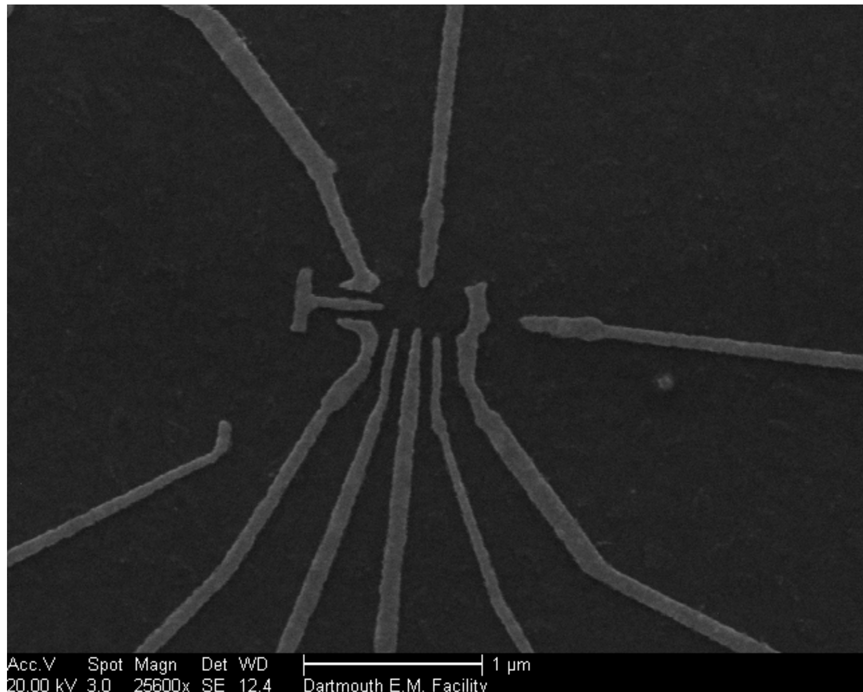


Figure 6.10 SEM micrograph of a double QD device pattern fabricated as part of a dose array on scrap material. Using dose arrays, a reliable lithography recipe for producing these double QD patterns was obtained.

6.5 Summary

This chapter presented results from measurements of a variety of devices fabricated on and in Si/SiGe heterostructures. A working RF-SET was achieved on Si/SiGe 2DEG material, and its performance

was consistent with similar devices fabricated on GaAs 2DEG substrates. QPCs were formed in Si/SiGe 2DEGs and the current leakage from the Schottky gates forming them affected their pinch-off performance. The addition of barrier oxides improved QPC performance and enabled formation of a QD. Integrated devices combining a QD and an RF-SET have been designed and fabricated, although one with a working RF-SET has not yet been achieved. Future devices will draw upon lithography recipes already developed that include both RF-SET and QPC charge sensors with a double QD device.

Chapter 7

Summary and Future Directions

This final chapter presents a brief summary of the material from the previous chapters, followed by a brief discussion of conclusions, before finishing with some comments regarding future directions.

7.1 Summary

Solid-state quantum dot qubits represent one of the most physically and economically viable approaches to a quantum computer. Spin-based quantum information in Si-based solid-state qubits is expected to have a longer lifetime than in GaAs-based systems. With GaAs devices serving as a proving ground, rapid progress in Si/SiGe heterostructure devices has been achieved. Based on that prior work and the theoretical understanding of mesoscopic devices presented in chapter 2, this work sought to develop modified fabrication processes that addressed materials issues specific to Si/SiGe systems that reduced overall device yield. A thorough presentation of experimental methods used in this work appeared in chapter 3, while the details and results the changes implemented to address materials issues appeared in chapters 4 and 5.

In particular, chapter 4 presented the results of investigations into three different ohmic contact

growth methods, including a discussion of the relevant parts of the theory of diffusion and alloying in Si. The results of experiments with depositing barrier oxides between the Schottky gates and the surface of the etched Si/SiGe device were presented in chapter 5. Data from a variety of devices appeared in chapter 6, including the realization of an RF-SET on Si/SiGe, the performance of QPCs with and without barrier oxides, and the formation of a QD in Si/SiGe with barrier oxides in place under the Schottky gates. Chapter 6 also included a discussion of the groundwork already paving the way towards integrated devices that combine RF-SET and QPC charge detectors with double QD systems.

7.2 Conclusions

The work presented here includes results from a host of experiments that shed new light on several aspects of quantum dots in Si/SiGe systems. Specifically, this work highlights several modifications to device fabrication sequence that, when implemented, result in better performance overall. Development of a robust ohmic contact growth process with yield approaching 100% eliminates a major issue that plagued earlier generations of devices with unreliability.

The unpredictable current leakage behavior frequently exhibited by Schottky gates used to form QPC and QD devices represents another hurdle to high yield in device fabrication. This work strongly suggests that the leakage current originates primarily from the sidewall region of the etched device mesa and that it can be controllably reduced by the deposition of a barrier oxide to cover this vulnerable region with an insulator. Implementing these changes required the development of new steps in the device fabrication procedure, and measurements on devices fabricated using these new methods indicate that the fundamental behaviors of QPCs and QDs in Si/SiGe are not altered by the presence of barrier oxide layers. Additionally, proof-of-priniciple experiments with the RF-SET on Si/SiGe suggests that this device can serve as a readout mechanism for QDs in this material,

much as it already does in the case of GaAs. Initial steps toward integrating RF-SETs with QDs in Si/SiGe are complete, as are the foundations for double QD devices integrating both RF-SETs and QPCs as charge detectors.

7.3 Future Directions

The results of the experiments presented here suggest that future directions for this work should focus on three major topics. First, and perhaps foremost, continuing work with the current device design will soon yield an integrated QD/RF-SET device, allowing for direct demonstration of charge sensing measurements. With only slight changes, the lithographic misalignment weakening the insulative effects of the barrier oxide is easily eliminated; these changes to the procedure already appear in the step-by-step fabrication sequence in Appendix A. The exploration of other insulator materials to serve as barrier oxides would also bear fruit, since the current SiO_2 films deposited by e-beam evaporation are not of the highest quality. In particular, Al_2O_3 films present a promising alternative, given their relative ease of deposition and more robust properties, both chemical and physical, when compared to SiO_2. Finally, the ultimate goal of this research direction includes the realization of qubit operations in Si/SiGe quantum dots. This goal requires continuing progress towards double QD devices with integrated readout mechanisms, and this work includes the initial steps in developing the lithography recipes required for those devices.

Appendix A

Step-by-Step Device Fabrication

This appendix provides a complete listing of the device fabrication sequence. Further details on each specific process can be found by referring to chapter 3.

1. Cleave sample chip from original wafer and sonicate in acetone for at least 10 minutes. Upon removal from acetone, rinse 3-5 seconds in isopropanol (IPA) and blow dry with pure dry nitrogen gas.

2. In the cleanroom, spin-coat sample with Shipley 1813 resist (a positive photoresist), using 500 rpm for 5 seconds, followed by 4000 rpm for 45 seconds. Be sure to place chips off-center on spinner stage to limit edge-bead to one side of sample.

3. Bake sample on bare hotplate surface for 2 minutes at 90°C.

4. Prepare mask aligner: load appropriate photomask and focus microscope on the etch pattern section of the mask. Load sample onto mask aligner stage.

5. Slowly raise stage until sample surface barely comes into focus, allowing room to adjust stage position to align pattern to sample.

6. Once aligned, raise sample into firm contact with the mask and expose to UV source for 14 seconds.

7. Develop pattern in MF-321 developer (a metal-free organic base solution) for 45 seconds, followed by a rinse in deionized water. Blow sample dry with pure dry nitrogen gas.

8. Prepare reactive ion etch (RIE) machine for device etching by setting the mass flow controllers to $\sim$12.5 for CF_4 gas and $\sim$0.7 for O_2 gas (a ratio approaching 20:1). This will yield an operating pressure of $\sim$100 mTorr when the plasma chamber is properly tuned. Adjust Forward Power setting to 100 W.

9. Run RIE process for 3-5 minutes on empty chamber twice, pumping out to high vacuum again between runs and adjusting the tuning knob to ensure that chamber is properly tuned (Reflected Power is minimized) in advance of etching the sample.

10. Run RIE process (100 W power, 100mT of CF_4/O_2[5%]), on real sample for 25 seconds to achieve etch depth of 100$\pm$15 nm.

11. Load sample into e-beam evaporator, pump out chamber to $\sim 5\times10^{-6}$ Torr, and deposit 70 nm of SiO_2.

12. Complete evaporation and place sample in covered acetone bath for at least 1.5 hours to lift off photoresist. To complete liftoff, sonicate in same acetone bath for 3-5 seconds, rinse for 3-5 seconds in IPA, and blow dry with pure dry nitrogen gas.

13. Repeat steps 3 through 8, using the ohmic contact pattern section of the photomask instead of the etch pattern.

14. Prepare three-source thermal evaporator in advance by pre-loading source materials: Au, Sb, and Au.

15. Dip sample in buffered oxide etch solution (BOE, a diluted aqueous mixture of HF and NH_4OH) for at least 15 seconds to remove native SiO_2 from surface.

16. As quickly as possible (¡ 2 minutes), load sample into thermal evaporator and immediately begin pumpdown.

17. When pressure reaches $\sim 5\times10^{-6}$ Torr, proceed with evaporation, depositing first 10 nm Au, then 1-2 nm Sb, followed by 70 nm Au.

18. Complete evaporation and place sample in covered acetone liftoff for at least 1.5 hours. To complete liftoff, sonicate in same acetone bath for 3-5 seconds, rinse for 3-5 seconds in IPA, and blow dry with pure dry nitrogen gas.

19. Anneal ohmic contacts using the strip heater. Begin by loading sample into strip heater and flushing chamber for 3-5 minutes with reducing gas mixture (20 percent H_2, balance of nonreactive gas, usually He, Ar, or N_2). Anneal for 1 minute at 110°C to remove any adsorbed water, followed by 4 minutes at 410°C to grow the ohmic contacts.

20. Repeat steps 3 through 8, using the Schottky gate leads pattern section of the photomask instead of the etch pattern.

21. Load sample into e-beam evaporator, pump out chamber to $\sim 5\times10^{-6}$ Torr, and deposit 30 nm of SiO_2, followed by 2-3 nm of Ti, and finally 90 nm of Pd.

22. Complete evaporation and place sample in covered acetone liftoff for at least 1.5 hours. To complete liftoff, sonicate in same acetone bath for 3-5 seconds, rinse for 3-5 seconds in IPA, and blow dry with pure dry nitrogen gas.

23. Image sample under optical microscope, noting the offset between the mesa formed by the etch and the Schottky gate leads so that it can be compensated for during later e-beam lithography

steps.

24. Prepare sample for e-beam lithography by affixing it to 1 cm square brass plate. Spin-coat brass plate with old e-beam resist for 10 seconds at 1000 rpm. Bake on hotplate for 3-5 minutes at 90°C

25. Spin-coat sample with PMMA 495 e-beam resist at 4000 rpm for 30 seconds and bake for 5-10 minutes at 180°C.

26. Spin-coat sample with PMMA 950 e-beam resist at 4000 rpm for 30 seconds and bake for 5-10 minutes at 180°C.

27. Using the SEM, expose Schottky gates e-beam pattern, taking into account the offset measured in step 22 above. The goal is to overlap the e-beam pattern with the photo pattern for the Schottky gates while also avoiding exposing the region near the edge of the mesa to ensure the barrier oxide remains intact.

28. Develop pattern by immersing sample in MIBK/IPA mixture (methylisobutyleketone, also known as 4-methyl-2-pentanone, 3:1 ratio by volume) for 60 seconds, followed by 40 seconds immersion in pure IPA, finishing by blowing dry with pure dry nitrogen.

29. Prepare RIE machine for native SiO_2 removal by setting the mass flow controller to ∼13.0 for CF_4 gas. This will yield an operating pressure of ∼100 mTorr when the plasma chamber is properly tuned. Adjust Forward Power setting to 25 W.

30. Run RIE process for 3-5 minutes on empty chamber twice, pumping out to high vacuum again between runs and adjusting the tuning knob to ensure that chamber is properly tuned (Reflected Power is minimized) in advance of exposing the sample.

31. Prepare e-beam evaporator in advance so that sample can be placed under vacuum immediately after removal from RIE process. Vent chamber and load Pd source.

32. Remove sample from brass plate and run RIE process (25 W power, 100mT of CF_4) on sample for 20 seconds to remove native oxide layer (a few nm thick).

33. After removal from the RIE chamber, immediately place sample into e-beam evaporator and begin pumpdown. When chamber pressure has reached $\sim 2\times 10^{-6}$ Torr, deposit 60 nm Pd.

34. Complete evaporation and place sample in covered acetone liftoff for at least 6 hours (preferably overnight). To complete liftoff, sonicate in same acetone bath for 3-5 seconds, rinse for 3-5 seconds in IPA, and blow dry with pure dry nitrogen gas.

35. Prepare sample for e-beam lithography by affixing it to 1 cm square brass plate. Spin-coat brass plate with old e-beam resist for 10 seconds at 1000 rpm. Bake on hotplate for 3-5 minutes at 90°C

36. Spin-coat sample with PMMA 495 e-beam resist at 4000 rpm for 30 seconds and bake for 5-10 minutes at 180°C.

37. Spin-coat sample with PMMA 495 e-beam resist at 4000 rpm for 30 seconds and bake for 5-10 minutes at 180°C.

38. Pre-expose lower layers of resist by illuminating with UV lamp for 10 minutes.

39. Spin-coat sample with PMMA 950 e-beam resist at 4000 rpm for 30 seconds and bake for 5-10 minutes at 180°C.

40. Using the SEM, expose SET e-beam pattern, taking into account the offset measured in step 22 above.

41. Develop pattern by immersing sample in MIBK/IPA mixture (methylisobutyleketone, also known as 4-methyl-2-pentanone, 3:1 ratio by volume) for 60 seconds, followed by 40 seconds immersion in pure IPA, finishing by blowing dry with pure dry nitrogen.

42. Prepare reactive ion etch (RIE) machine for de-scumming O_2 plasma cleaning by setting the mass flow controller to $\sim$13.0 for O_2 gas. This will yield an operating pressure of $\sim$100 mTorr when the plasma chamber is properly tuned. Adjust Forward Power setting to 25 W.

43. Run RIE process for 3-5 minutes on empty chamber once, adjusting the tuning knob to ensure that chamber is properly tuned (Reflected Power is minimized) in advance of exposing the sample.

44. Run RIE process (25 W power, 100mT of CF_4) on sample for 20 seconds to remove resist residue, ensuring reliable metal-to-metal contact between subsequent layers.

45. Place sample into two-source thermal evaporator, loaded with Al metal in both sources (5 pellets in source A, 6 pellets in source B).

46. Once chamber pressure reaches $\sim 1\times 10^{-6}$ Torr, perform shadow evaporation to create SET, depositing 20 nm Al for the first layer.

47. Form aluminum oxide for the tunnel junctions by allowing 100-110 mTorr of O_2 mixture into chamber for 3 minutes after sealing the high vacuum valve. (Oxidation recipes are known to vary quite a bit.)

48. Tilt sample by rotating the tilt control 22-23 turns between layers. After tilting, deposit 40 nm Al for the second layer.

49. Complete evaporation and place sample in covered acetone liftoff for at least 6 hours (preferably overnight). To complete liftoff, sonicate in same acetone bath for 3-5 seconds, rinse for 3-5

seconds in IPA, and blow dry with pure dry nitrogen gas.

50. Affix sample to appropriate apparatus, wirebond, and measure.

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